# **9深圳广宁** 广宁伟业液晶显示有限公司

## **PRODUCT SPECIFICATIONS**

For Custor	mer:	: APPRO	: APPROVAL FOR SPECIFICATION				
Customer I	Model	]	☐ : APPROVAL FOR SAMPLE				
No. <u>GN070QPH4007118W</u>		<u>18W</u>	Date	: 2021.	1 1.04		
Module No.:			Versi	on : A			
1. Table	of Conte	nts					
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## 2. Revision Record

Date	Rev.No.	Page	Revision Items	Prepared
2021.11.04	Α		初版	

## 3. General Specifications

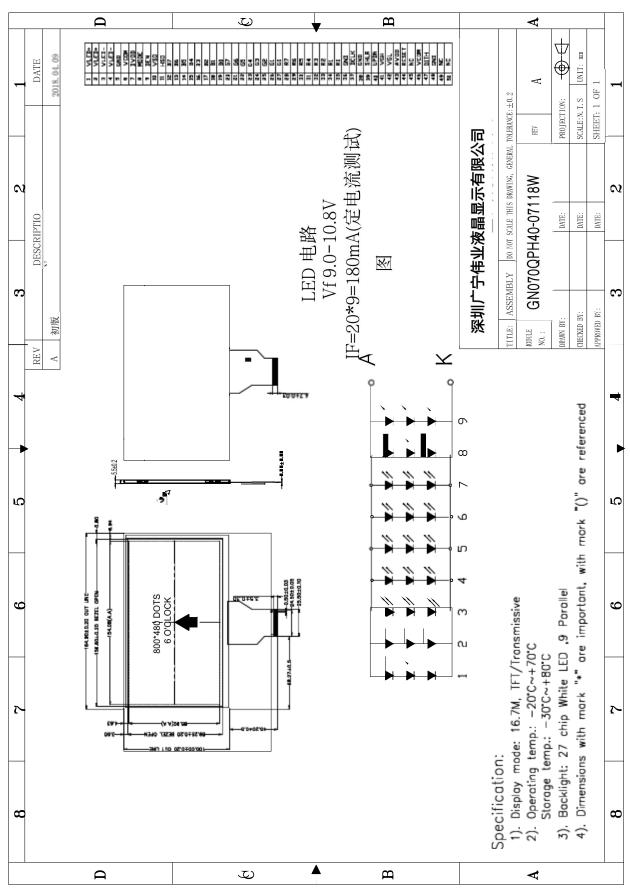
GN070QPH40-07118W is a TFT-LCD module. It is composed of a TFT-LCD panel, driver IC, FPC, a back light unit. The 7.0" display area contains 800 x 480 pixels and can display up to 16.7M colors. This product accords with RoHS environmental criterion.

Item	Contents	Unit	Note
LCD Type	Normally White,Transmissive	-	
Display color	16.7M		1
Viewing Direction	6	O'Clock	
Operating temperature	-10~+60	°C	
Storage temperature	-20~+70	င	
Module size	164.90(W)×100.00(H)×5.50(T)	mm	2
Active Area(W × H)	154.08(W)×85.92(H)	mm	
Number of Dots	800× RGB×480	dots	
Backlight	27-LEDs (white)	pcs	
Interface	RGB Interface	-	

Note 1: Color tune is slightly changed by temperature and driving voltage.

Note 2: Without FPC and Solder.

## 4. Outline. Drawing



## 5. Absolute Maximum Ratings(Ta=25°C)

#### 5.1 Electrical Absolute Maximum Ratings.(Vss=0V,Ta=25°C)

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	Vcc	-0.3	3.6	V	
Logic Signal Input /Output Voltage	Viovec	-0.3	Vcc+0.5	V	4 2
Power Supply Voltage for LCD	Vop	0	2.8	V	1, 2
Current of LED	ILED	0	60	mĄ	

#### Notes:

- If the module is above these absolute maximum ratings. It may become permanently damaged.
   Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.
- 2.  $V_{CC} > V_{SS}$  must be maintained.
- 3. Please be sure users are grounded when handing LCD Module.

#### 5.2 Environmental Absolute Maximum Ratings.

Item	Stor	age	Opera	Note	
пеш	MIN.	MAX.	MIN.	MAX.	Note
Ambient Temperature	-20°C	<b>70</b> ℃	- 10°C	60°C	1,2
Humidity	-	-	-	-	3

- 1. The response time will become lower when operated at low temperature.
- 2. Background color changes slightly depending on ambient temperature.

  The phenomenon is reversible.
- 3. Ta<=40°C:85%RH MAX.

Ta>=40°C:Absolute humidity must be lower than the humidity of 85%RH at 40°C.

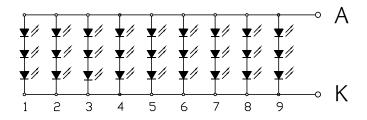
## **6. Electrical Specifications and Timing Characteristics**

#### 6.1 Electrical characteristics(Vss=0V ,Ta=25°C)

Item	Symbol	Min.	Тур	Max.	Unit
Digital Supply Voltage	DVDD	3.0	3.3	3.6	V
Analog Supply Voltage	AVDD		9.6		V
TFT Gate ON Voltage	VGH	14.5	15	15.5	V
TFT Gate OFF Voltage	VGL	-10.5	- 10	-9.5	V
TFT Common Electrode Voltage	VCOM	3.84	4.04	4.24	V

## 6.2 LED backlight specification(VSS=0V ,Ta=25℃)

Item	Symbol	Condition	Min	Тур	Max	Unit	Note
Supply voltage	-	-	9.0	9.6	10.8	V	1
Supply current	lf	-	-	180	-	mΑ	2



#### Note:

1: VLED=VLED(+)-VLED(-).

2:The current of LED is 20mA.

A LED drive in constant current mode is recommended.

#### 6.3 Interface signals

1-2	Pin NO.	SYMBOL	DESCRIPTION			
5 GND Power ground 6 VCOM Common Voltage 7 DVDD Digital Power  B DE/SYNC mode select. Normally pull high. H: DE mode. L: HSD/VSD mode.  9 DEN Data Enable signal 10 VSD Vertical sync input 11 HSD Horizontal sync input 11 HSD Horizontal sync input 12~19 B7~B0 If you use 18-bit.please use B7-B2,and connect B0-B1 to GND Green Data Input, If you use 18-bit.please use G7-G2,and connect G0-G1 to GND Red Data Input, If you use 18-bit.please use R7-R2,and connect R0-R1 to GND A6 GND Power ground 36 GND Power ground 37 DCLK Clock input 38 GND Power ground 39 SHLR Left or Right Display Control 40 UPDN Up / Down Display Control 41 VGH Positive Power for TFT 42 VGL Negative Power for TFT 43 AVDD Analog Power 44 RESET Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high. 45 NC Not connection DITH—"H", enable internal dithering function DITH—"H", disable internal dithering function DITH—"H", disable internal dithering function DITH—"I", disable internal dithering function DITH—"I", disable internal dithering function	1~2	VLED+	Power for LED backlight (Anode)			
6 VCOM Common Voltage 7 DVDD Digital Power  B DE/SYNC mode select. Normally pull high.  H: DE mode. L: HSD/VSD mode.  9 DEN Data Enable signal  10 VSD Vertical sync input  11 HSD Horizontal sync input  12~19 B7~B0 Blue Data Input, If you use 18-bit,please use B7-B2,and connect B0-B1 to GND  28~35 R7~R0 Green Data Input, If you use 18-bit,please use G7-G2,and connect G0-G1 to GND  28~35 R7~R0 Red Data Input, If you use 18-bit,please use R7-R2,and connect R0-R1 to GND  36 GND Power ground  37 DCLK Clock input  38 GND Power ground  39 SHLR Left or Right Display Control  40 UPDN Up / Down Display Control  41 VGH Positive Power for TFT  42 VGI. Negative Power for TFT  43 AVDD Analog Power  44 RESET Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high.  NC Not connection  VCOM Common Voltage  Dithering function enable control.  DITH="IT", chable internal dithering function DITH="IT", disable internal dithering function DITH="IT", chable internal dithering function DITH="IT", disable internal dithering function DITH="IT", disable internal dithering function	3~4	VLED-	Power for LED backlight (Cathode)			
7 DVDD Digital Power  B DE/SYNC mode select. Normally pull high.  H: DE mode. L: HSD/VSD mode.  9 DEN Data Enable signal  10 VSD Vertical sync input  11 HSD Horizontal sync input  12~19 B7~B0 Blue Data Input, If you use 18-bit, please use B7-B2, and connect B0-B1 to GND  Green Data Input, If you use 18-bit, please use G7-G2, and connect G0-G1 to GND  Red Data Input, If you use 18-bit, please use R7-R2, and connect R0-R1 to GND  Red Data Input, If you use 18-bit, please use R7-R2, and connect R0-R1 to GND  36 GND Power ground  37 DCLK Clock input  38 GND Power ground  39 SHLR Left or Right Display Control  40 UPDN Up / Down Display Control  41 VGH Positive Power for TFT  42 VGL Negative Power for TFT  43 AVDD Analog Power  44 RESET Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high.  NC Not connection  VCOM Common Voltage  Dithering function enable control.  DITH="It", enable internal dithering function DITH="It", disable internal dithering function DITH="L", disable internal dithering function	5	GND	ower ground			
BE/SYNC mode select. Normally pull high. H: DE mode. L: HSD/VSD mode.  9 DEN Data Enable signal  10 VSD Vertical sync input  11 HSD Horizontal sync input  12~19 B7~B0 Blue Data Input, If you use 18-bit,please use B7-B2,and connect B0-B1 to GND  Green Data Input, If you use 18-bit,please use G7-G2,and connect G0-G1 to GND  28~35 R7~R0 Red Data Input, If you use 18-bit,please use R7-R2,and connect R0-R1 to GND  36 GND Power ground  37 DCLK Clock input 38 GND Power ground  39 SHLR Left or Right Display Control  40 UPDN Up / Down Display Control  41 VGH Positive Power for TFT  42 VGL Negative Power for TFT  43 AVDD Analog Power  44 RESET Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high.  NC Not connection  DITH="It", enable internal dithering function DITH="It", disable internal dithering function	6	VCOM	ommon Voltage			
8 MODE L: HSD/VSD mode.  9 DEN Data Enable signal  10 VSD Vertical sync input  11 HSD Horizontal sync input  12~19 B7~B0 Blue Data Input, 1f you use 18-bit, please use B7-B2, and connect B0-B1 to GND  20~27 G7~G0 Green Data Input, 1f you use 18-bit, please use G7-G2, and connect G0-G1 to GND  Red Data Input, 1f you use 18-bit, please use G7-G2, and connect G0-G1 to GND  Red Data Input 1f you use 18-bit, please use R7-R2, and connect R0-R1 to GND  36 GND Power ground  37 DCLK Clock input  38 GND Power ground  39 SHLR Left or Right Display Control  40 UPDN Up / Down Display Control  41 VGH Positive Power for TFT  42 VGL Negative Power for TFT  43 AVDD Analog Power  44 RESET Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high.  45 NC Not connection  46 VCOM Common Voltage  Dithering function enable control.  DITH="\text{"T," disable internal dithering function}  DITH="\text{"T," disable internal dithering function}  Power ground.  49 NC Not connection	7	DVDD	Digital Power			
10 VSD Vertical sync input  11 HSD Horizontal sync input  12~19 B7~80 Blue Data Input, 1f you use 18-bit,please use B7-B2,and connect B0-B1 to GND  20~27 G7~G0 Green Data Input, 1f you use 18-bit,please use G7-G2,and connect G0-G1 to GND  28~35 R7~R0 Red Data Input 1f you use 18-bit,please use R7-R2,and connect R0-R1 to GND  36 GND Power ground  37 DCLK Clock input  38 GND Power ground  39 SHLR Left or Right Display Control  40 UPDN Up / Down Display Control  41 VGH Positive Power for TFT  42 VGL Negative Power for TFT  43 AVDD Analog Power  44 RESET Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high.  45 NC Not connection  DITH="H", enable internal dithering function DITH="H", enable internal dithering function  DITH="L", disable internal dithering function  DITH="L", disable internal dithering function  Power ground.  49 NC Not connection	8	MODE	H: DE mode.			
11 HSD Horizontal sync input  12-19 B7-B0 Blue Data Input, If you use 18-bit,please use B7-B2,and connect B0-B1 to GND  20-27 G7-G0 Green Data Input, If you use 18-bit,please use G7-G2,and connect G0-G1 to GND  28-35 R7-R0 Red Data Input If you use 18-bit,please use R7-R2,and connect R0-R1 to GND  36 GND Power ground  37 DCLK Clock input  38 GND Power ground  39 SHLR Left or Right Display Control  40 UPDN Up / Down Display Control  41 VGH Positive Power for TFT  42 VGL Negative Power for TFT  43 AVDD Analog Power  44 RESET Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high.  45 NC Not connection  46 VCOM Common Voltage  Dithering function enable control.  DITH="H", enable internal dithering function DITH="L", disable internal dithering function 48 GND Power ground.  49 NC Not connection	9	DEN	Data Enable signal			
B7-B0   Blue Data Input,   If you use 18-bit,please use B7-B2,and connect B0-B1 to GND	10	VSD	Vertical sync input			
12-19   B7-B0   If you use 18-bit, please use B7-B2, and connect B0-B1 to GND	11	HSD	Horizontal sync input			
20-27 G7-G0 If you use 18-bit,please use G7-G2,and connect G0-G1 to GND  Red Data Input If you use 18-bit,please use R7-R2,and connect R0-R1 to GND  36 GND Power ground  37 DCLK Clock input  38 GND Power ground  39 SHLR Left or Right Display Control  40 UPDN Up / Down Display Control  41 VGH Positive Power for TFT  42 VGL Negative Power for TFT  43 AVDD Analog Power  44 RESET Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high.  45 NC Not connection  46 VCOM Common Voltage  Dithering function enable control.  DITH="H", enable internal dithering function DITH="L", disable internal dithering function  48 GND Power ground.  Not connection	12~19	B7~B0				
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40 UPDN Up / Down Display Control  41 VGH Positive Power for TFT  42 VGL Negative Power for TFT  43 AVDD Analog Power  44 RESET Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high.  45 NC Not connection  46 VCOM Common Voltage  Dithering function enable control.  DITH DITH="H", enable internal dithering function DITH="L", disable internal dithering function  48 GND Power ground.  49 NC Not connection	38	GND	Power ground			
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42 VGL Negative Power for TFT  43 AVDD Analog Power  44 RESET Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high.  45 NC Not connection  46 VCOM Common Voltage  Dithering function enable control.  DITH="H", enable internal dithering function DITH="L", disable internal dithering function  48 GND Power ground.  49 NC Not connection	40	UPDN	Up / Down Display Control			
AVDD Analog Power  Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high.  NC Not connection  VCOM Common Voltage  Dithering function enable control.  DITH="H", enable internal dithering function DITH="L", disable internal dithering function  48 GND Power ground.  NC Not connection	41	VGH	Positive Power for TFT			
44 RESET Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high.  45 NC Not connection  46 VCOM Common Voltage  Dithering function enable control.  DITH="H", enable internal dithering function DITH="L", disable internal dithering function  48 GND Power ground.  49 NC Not connection	42	VGL	Negative Power for TFT			
an RC reset circuit for stability. Normally pull high.  NC Not connection  Common Voltage  Dithering function enable control.  DITH DITH="H", enable internal dithering function DITH="L", disable internal dithering function  RESET  an RC reset circuit for stability. Normally pull high.  NC Not connection	43	AVDD	Analog Power			
46 VCOM Common Voltage  Dithering function enable control.  DITH="H", enable internal dithering function  DITH="L", disable internal dithering function  48 GND Power ground.  49 NC Not connection	44	RESET				
Dithering function enable control.  DITH="H", enable internal dithering function  DITH="L", disable internal dithering function  GND Power ground.  NC Not connection	45	NC	Not connection			
47 DITH DITH="H", enable internal dithering function DITH="L", disable internal dithering function  48 GND Power ground.  49 NC Not connection	46	VCOM	Common Voltage			
49 NC Not connection	47	DITH	DITH="H", enable internal dithering function			
	48	GND	Power ground.			
50 NC Not connection	49	NC	Not connection			
	50	NC	Not connection			

### 7. Optical Characteristics

Item	Sy	mbol	Condition	Min.	Тур.	Max.	Unit	Note
Brightness	l	Зр	<i>θ</i> =0°	-	300	-	Cd/m <sup>2</sup>	1
Uniformity	Δ	Вр	Ф=0°	75	80		%	1,2
	3	:00		-	55	-		
Viewing	6	:00	Cr≥10	-	55	-	Deg	3
Angle	9	:00	GIZ 10	-	55	-	Deg	3
	12	2:00		-	40	-		
Contrast Ratio	(	Cr	<i>θ</i> =0°	400	500		-	4
Response Time	Т	·+T <sub>f</sub>	Ф=0°		35	50	ms	5
		Х		0.26	0.31	0.36	-	
	W	у		0.27	0.32	0.37	-	
		Υ		-	-	-		
	R	Х					-	
Color of		у					-	
Color of CIE		Υ		-	-	-		
Coordinate		Х	<i>θ</i> =0°				-	1,6
	G	у	Ф=0°				-	1,0
		Y		-	-	-		
		Х					-	
	В	у					-	
		Υ		-	-	-		
NTSC Ratio		S		-	50	-	%	

Note: The parameter is slightly changed by temperature, driving voltage and materiel

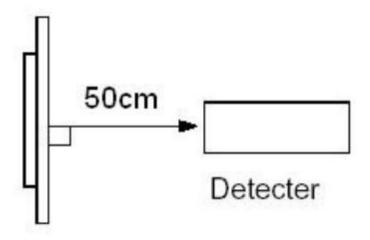
Note 1: The data are measured after LEDs are turned on for 5 minutes. LCM displays full white.

The brightness is the average value of 9 measured spots. Measurement equipment PR-705 (Φ8mm)

#### Measuring condition:

- Measuring surroundings: Dark room .
- Measuring temperature: Ta=25°C .
- Adjust operating voltage to get optimum contrast at the center of the display.

Measured value at the center point of LCD panel after more than 5 minutes while backlight turning on.

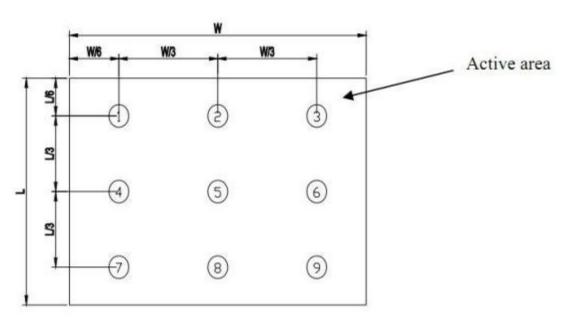


Note 2: The luminance uniformity is calculated by using following formula.

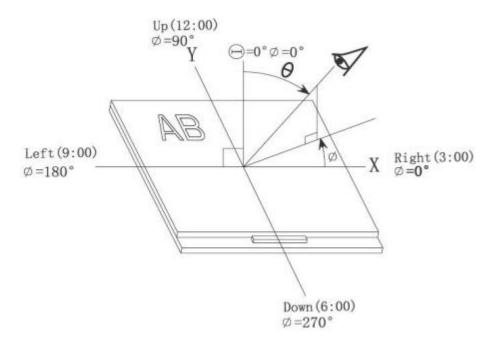
⊿Bp = Bp (Min.) / Bp (Max.)×100 (%)

Bp (Max.) = Maximum brightness in 9 measured spots

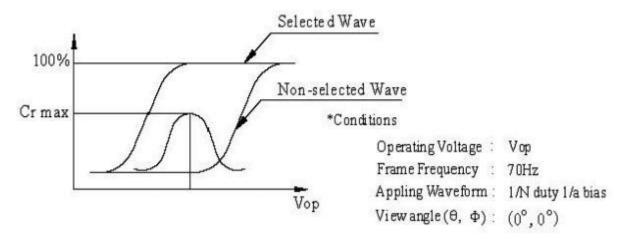
Bp (Min.) = Minimum brightness in 9 measured spots.



Note 3: The definition of viewing angle: Refer to the graph below marked by  $\theta$  and  $\Phi$ 



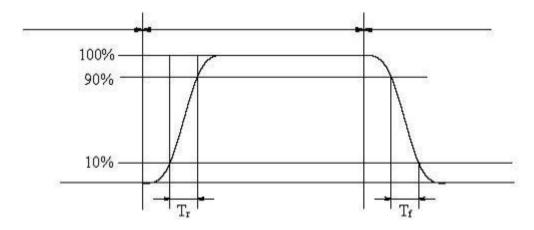
Note 4: Definition of contrast ratio.( Test LCD using DMS501)



$$Contrast\ ratio\ (\mathit{Cr}) = \frac{\mathit{Brightness}\ \mathit{of}\ \mathit{selected}\ \mathit{dots}}{\mathit{Brightness}\ \mathit{of}\ \mathit{non-selected}\ \mathit{dots}}$$

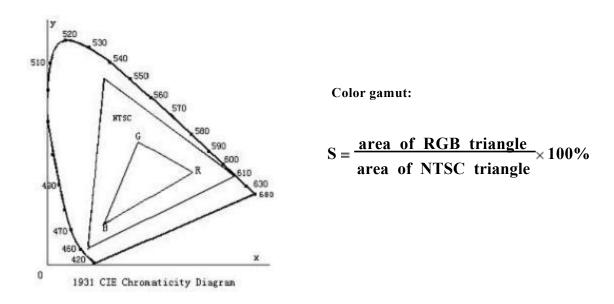
Note 5: Definition of Response time. (Test LCD using DMS501):

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (falling time) and from "white" to "black" (rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



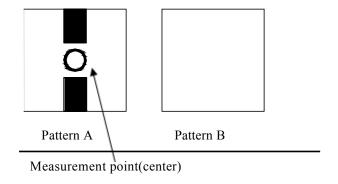
The definition of response time

Note 6: Definition of Color of CIE Coordinate and NTSC Ratio.



Note 7: Definition of cross talk.

Cross talk ratio(%)= |pattern A Brightness-pattern B Brightness|/pattern A Brightness\*100



Electric volume value=3F+/-3Hex

## 8. Reliability Test Items and Criteria

No	Test Item	Test condition	Criterion
1	High Temperature Storage	70°C±2°C 96H Restore 2H at 25°C Power off	
2	Low Temperature Storage	-20°C±2°C 96H Restore 2H at 25°C Power off	1. After testing,
3	High Temperature Operation	60°C±2°C 96H Restore 2H at 25°C Power on	cosmetic and electrical defects should not happen.
4	Low Temperature Operation	- 10°C±2°C 96H Restore 4H at 25°C Power on	2. Total current consumption should not be more than twice
5	High Temperature/Humidity Operation	40℃±2℃ 90%RH 96H Power on	of initial value.
6	Temperature Cycle(Storage)	20°C ←70°C  30min 5min 30min  after 5 cycle, Restore 2H at 25°C  Power off	
7	Vibration Test	10Hz~ 150Hz, 100m/s <sup>2</sup> , 120min	Not allowed cosmetic
8	Shock Test	Half- sine wave,300m/s <sup>2</sup> , 11ms	and electrical defects.
9	ESD Test	Air discharge:+/-8KV, Contact discharge:4KV	

Note: Operation: Supply 3.3V for logic system .

The inspection terms after reliability test, as below

ITEM	Inspection
Contrast	CR>50%
IDD	IDD<200%
Brightness	Brightness>60%
Color Tone	Color Tone+/-0,05

## 9 Quality level

#### 9.1 Classification of defects

Major defects (MA): A major defect refers to a defect that may substantially

degrade usability for product applications, including all functional defects(such as no display, abnormal display, open or missing segment, short circuit, missing component), outline dimension beyond the drawing, progressive defects and those affecting reliability.

Minor defects (MI): A minor defect refers to a defect which is not considered to be able to substantially degrade the product application or a defect that deviates from existing standards almost unrelated to the effective use of the product or its operation, such as black spot, white spot, bright spot, pinhole, black line, white line, contrast variation, glass defect, polarizer defect, etc.

#### 9.2 Definition of inspection range

For dot defect of TFT LCD which is not smaller than 3 inches, dividing three areas to make a judgment (according to figure 1).

A area: center of viewing area

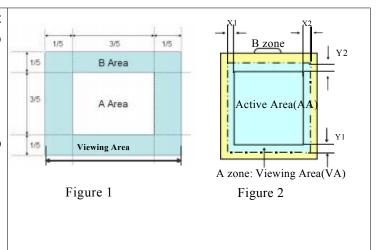
B area : periphery of viewing area

C area: Outside viewing area

For other defects, dividing two areas to make a judgment (according figure 2).

A zone : Inside Viewing area B zone : Outside Viewing area

X1(A.A~V.A): 2mm X2(A.A~V.A): 2mm Y1(A.A~V.A): 2mm Y2(A.A~V.A): 2mm



#### 9.3 Inspection items and general notes

General notes	1.Should any defects which are not specified in this standard happen, additional standard she determined by mutual agreement between customer and TIANMA.  2.Viewing area should be the area which TIANMA guarantees.  3.Limit sample should be prior to this Inspection standard.  4.Viewing judgment should be under static pattern.  5.Inspection conditions Inspection distance: 250 mm (from the sample) Inspection angle : 45 degrees in 6 o 'clock direction (all defects in viewing area should inspected from this direction)			
	Pinhole, Bright spot, Black spot, White spot, Black line, White Line, Foreign particle, Bubble	The color of a small area is different from the remainder. The phenomenon doesn't change with voltage		
Increation	Contrast variation	The color of a small area is different from the remainder. The phenomenon changes with voltage		
Inspection	Polarizer defect	Scratch, Dirt, Particle, Bubble on polarizer or between polarizer and glass		
	Dot defect (TFT LCD)	The pixel appears bright or dark abnormally when display		
	Functional defect	No display, Abnormal display, Open or missing segment, Short circuit, False viewing direction		

Glass defect	Glass crack, Shaved corner of glass, Surplus glass
PCB defect	Components assembly defect

## 9.4 Outgoing Inspection level

Outgoing Inspection	Inspection conditions	Inspection				
standard	inspection conditions	Min.	Max.	Unit	IL	AQL
Major Defects	See 8.3 general notes	See 8.5		II	0.065	
Minor Defects See 8.3 general notes		See 8.5		II	0.065	
Note: Sampling standard conforms to GB2828						

## 9.5 Inspection Items and Criteria

Inspection items			Judgment standard					
				Category	Acceptable number			
				Category	A zone	B zone		
	Black spot, White spot, Pinhole, Foreign Particle, Particle in or on glass, Scratch on glass	D b a Φ=(a+b)/2(mm	Α	Ф<=0.20	Neglected	Neglected		
			В	0.20<Ф<=0.25	3	Neglected		
1			С	0.25<Ф<=0.3	2	Neglected		
'			D	0.3<Ф<=0.4	1	3		
		(a/b<2.5)	E	0.4<Ф<=0.5	0	2		
			Tota	al defective point(B,C)	1	-		
	Black line, White line, and Particle Between Polarizer and glass, Scratch on glass	W: Width L:Length(mm) L/W>=2.5	A	W<=0.03	Neglected	Neglected		
			В	0.03 <w<=0.05 L&lt;=3.0</w<=0.05 	3	Neglected		
2			С	0.05 <w<=0. 1<br="">L&lt;=3.0</w<=0.>	2	Neglected		
2			D	0.05 <w<=0. 1<br="">L&lt;=4.0</w<=0.>	1	3		
			Е	W>0. 1 L>4.0	0	2		
			Total defective point(B,C)		1	-		
3	3 Bright spot			any size	none	none		
4	Contrast		А Ф<0.2		Neglected	Neglected		

	variation		В	0.2<Ф<=0.3	2				
		$ \begin{array}{c} b\\ \hline a\\ \Phi=(a+b)/2(mm) \end{array} $	С	0.3<Ф<=0.4					
			D	0.4<Ф	0				
			Total defective point(B,C)		3				
5	Bubble inside cell		any size none none						
	Polarizer defect	Scratch ,damage on polarizer, Particle on polarizer or between polarizer and glass.	Refer to item 1 and item 2.						
6	(if Polarizer is used)	Bubble, dent and convex	Α	Ф<=0. 1	Neglected	Neglected			
	,		В	0. 1 <Ф<=0.2	2	Neglected			
			С	0.2 <Ф<=0.3	1	2			
7	Surplus glass	Surrounding surplus glass	B<=0.3mm  Should not influence outline dimension and assembling.						
8	Open segment or open common			Not permitted					
9	Short circuit			Not permitted					
10	False viewing direction			Not permitted					
11	Contrast ratio uneven			According to the limit specimen					
12	Crosstalk			According to the limit specimen					
13	Black /White spot(display)			Refer to item 1					
14	Black /White line(display)			Refer to item 2					

			Judgment standard			
		Inspection items		Category(application: B zone)	Acceptable number	
		i )The front of lead terminals	A	a≤ t, b≤1/5W, c≤3mm		
	Glass defect crack	b c c	В	Crack at two sides of lead terminals should not cover patterns and alignment mark		
		ii )Surroundin seal ack-non-contact side  c b a t  Inner border line of the seal  Outer border line of the seal	b·	Inner borderline of the seal	Max.3 defects allowed	
15		Inner border line of the seal Outer border line of the seal	b	< Outer borderline of the seal		
		iv)Corner  a t		a <= t, b <= 3.0, c <= 3.0  Glass crack should not cover patterns u and alignment mark and patterns.		

Inspection items			Judgment standard			
		inspection items	Category(application: B zone)			
16	PCB defect	Component soldering: No cold soldering 、short 、open circuit、burr 、tin ball The flat encapsulation component position deviation must be less than 1/3 width of the pin (Pic. 1); the sheet component deviation: Pin deviates from the pad and contact with the near components is not permitted (Pic.2)  lead defect: The lead lack must be less than 1/3 of its width; The lead burr must be less than 1/3 of the seam; Impurities connect with the near leads is not permitted	Component Soldering pad Lead L2>0  L1>0			
		Connector soldering: Soldering tin is at contact position of the plug and socket is not permitted No foundation is scald Serious cave distortion on plug and socket contact pin is not permitted  Glue on root of the speaker receiver and motor lead: The insulative cost of the lead must join	Soldering tin is not permit in this area  Soldering tin is not permit in this area  Socket  Base Board			
		The insulative coat of the lead must join into the PCB; the protected glue must envelop to the insulative coat.	PCB Insulative coat			

#### 10. Precautions for Use of LCD Modules

#### **10.1 Handling Precautions**

- 10. 1. 1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- 10. 1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.
- 10. 1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- 10. 1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
- 10. 1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:
  - Isopropyl alcohol
  - Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents
- 10. 1.6 Do not attempt to disassemble the LCD Module.
- 10. 1.7 If the logic circuit power is off, do not apply the input signals.
- 10. 1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
  - a. Be sure to ground the body when handling the LCD Modules.
  - b. Tools required for assembly, such as soldering irons, must be properly ground.
  - c. To reduce the amount of static electricity generated, do not conduct

assembly and other work under dry conditions.

d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

#### 10.2 Storage precautions

- 10.2. 1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.
- 10.2.2 The LCD modules should be stored under the storage temperature range.
  If the LCD modules will be stored for a long time, the recommend condition is:

Temperature :  $0 \,^{\circ}\text{C} \sim 40 \,^{\circ}\text{C}$ 

Relatively humidity: ≤80%

- 10.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.
- 10.3 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.