MCP Specification

128Mb NOR Flash + 32Mb UtRAM

Document Title

Multi-Chip Package MEMORY

128M Bit(8M x16) Page Mode, Multi Bank NOR Flash /

32M Bit(2M x16) Page Mode Uni-Transistor Random Access Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial issue. - NOR Flash 128Mb B-die Ver_0.9 - UtRAM 32Mb D-die Ver_1.0	Sep. 11, 2006	Preliminary

Note : For more detailed features and specifications including FAQ, please refer to Samsung's web site.
http://samsungelectronics.com/semiconductors/products/products_index.html

Multi-Chip Package MEMORY

128M Bit(8M x16) Page Mode, Multi Bank NOR Flash /
32M Bit(2M x16) Page Mode Uni-Transistor Random Access Memory

FEATURES

<Common>
- Operating Temperature : -25°C ~ 85°C
- Package : 64Ball FBGA _ 8.0mm x 11.6mm x 1.2mmt
  0.8mm ball pitch

<NOR Flash>
- Single Voltage, 2.7V to 3.6V for Read and Write operations
  Voltage range of 2.7V to 3.1V valid for MCP product
- Organization
  8M x16 bit (Word mode Only)
- Fast Read Access Time : 55ns
- Page Mode Operation
  8 Words Page access allows fast asychronous read
  Page Read Access Time : 20ns
- Read While Program/Erase Operation
- Multiple Bank architectures (4 banks)
  Bank 0: 16Mbit (4Kw x 8 and 32Kw x 31)
  Bank 1: 48Mbit (32Kw x 96)
  Bank 2: 48Mbit (32Kw x 96)
  Bank 3: 16Mbit (4Kw x 8 and 32Kw x 31)
- OTP Block : Extra 256 word
  - 128word for factory and 128word for customer OTP
- Power Consumption (typical value)
  - Active Read Current : 45mA (@10MHz)
  - Program/Erase Current : 17mA
  - Read While Program or Read While Erase Current : 35mA
  - Standby Mode/Auto Sleep Mode : 15uA
- Support Single & Quad word accelerate program
- $\overline{WP}$/ACC input pin
  - Allows special protection of two outermost boot blocks at V_{IL}, regardless of block protect status
  - Removes special protection of two outermost boot block at V_{IH}, the two blocks return to normal block protect status
  - Reduce program time at V_{HH} : 4us/word
  - Accelerated Quadword Program time : 1.2us
- Erase Suspend/Resume
- Program Suspend/Resume
- Unlock Bypass Program
- Hardware $\overline{RESET}$ Pin
- Command Register Operation
- Block Protection / Unprotection
- Supports Common Flash Memory Interface

<UtRAM>
- Process Technology: CMOS
- Organization: 2M x16 bit
- Power Supply Voltage: 2.7~3.1V
- Three State Outputs
- Compatible with Low Power SRAM
- Support 4 page read mode

GENERAL DESCRIPTION

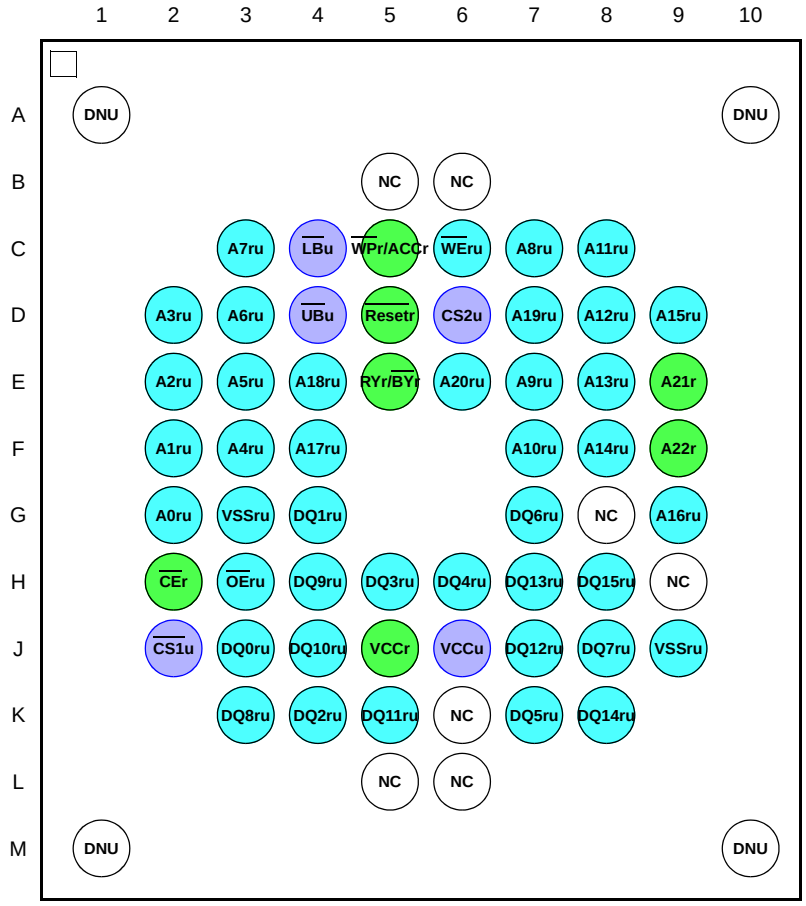
The K5L2731CAM is a Multi Chip Package Memory which combines 128Mbit NOR Flash Memory and 32Mbit Page UtRAM.

The NOR Flash featuring single 3.0V power supply, is an 128Mbit NOR-type Flash Memory organized as 8M x16. The memory architecture of the device is designed to divide its memory arrays into 270 blocks with independent hardware protection. This block architecture provides highly flexible erase and program capability. The NOR Flash consists of four banks. This device is capable of reading data from one bank while programming or erasing in the other banks. The NOR Flash offers fast page access time of 20~30ns with random access time of 55~70ns. The device's fast access times allow high speed microprocessors to operate without wait states. The device performs a program operation in unit of 16 bits (Word) and erases in units of a block. Single or multiple blocks can be erased. The block erase operation is completed within typically 0.7 sec. The device requires 15mA as program/erase current in the commercial and industrial temperature ranges.

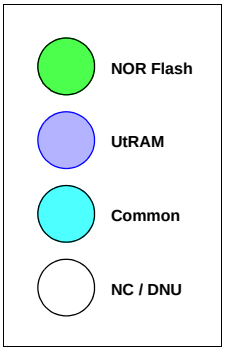
The 32Mb UtRAM is fabricated by SAMSUNG's advanced CMOS technology using one transistor memory cell. The device support 4 page mode operation, Industrial temperature range and 48 ball Chip Scale Package for user flexibility of system design. The device also supports Internal Temperature Compensated Self Refresh for low standby current.

The K5L2731CAM is suitable for the memory of mobile communication system to reduce not only mount area but also power consumption. This device is available in 64-ball FBGA package.

PIN CONFIGURATION



64 FBGA: Top View (Ball Down)



PIN DESCRIPTION

Ball Name	Description	Ball Name	Description
A0ru to A20ru	Address Inputs(Common)	$\overline{WE}$ru	Write Enable(Common)
A21r to A22r	Address Inputs(NOR)	$\overline{UB}$u	Upper Byte(UtRAM)
DQ0ru to DQ15ru	Data Input/output(Common)	$\overline{LB}$u	Lower Byte(UtRAM)
$\overline{CE}$r	Chip Enable (NOR)	VCCr	Power Supply(NOR)
$\overline{CS}$1u,CS2u	Chip Select (UtRAM)	VCCu	Power Supply(UtRAM)
$\overline{OE}$ru	Output Enable (Common)	VSSru	Ground(Common)
$\overline{RESET}$r	Hardware Reset (NOR)	NC	No Connection
$\overline{WP}$r/ACCr	Hardware Write Protection/ Program Acceleration(NOR)	DNU	Do Not Use
RYr/$\overline{BY}$r	Ready/Busy Output(NOR)		

ORDERING INFORMATION

K 5 L 27 31 C A M - D 7 70

Samsung MCP Memory
2Chip MCP

Device Type
L : De-muxed NOR Flash + UtRAM

NOR Flash Density
27 : 128Mb, x16 ,Page, 1CE

UtRAM Density, (Organization)
31 : 32Mb, x16, Page

Operating Voltage
C : 3.0V/3.0V

Block Architecture
A : Top & Bottom Boot Block

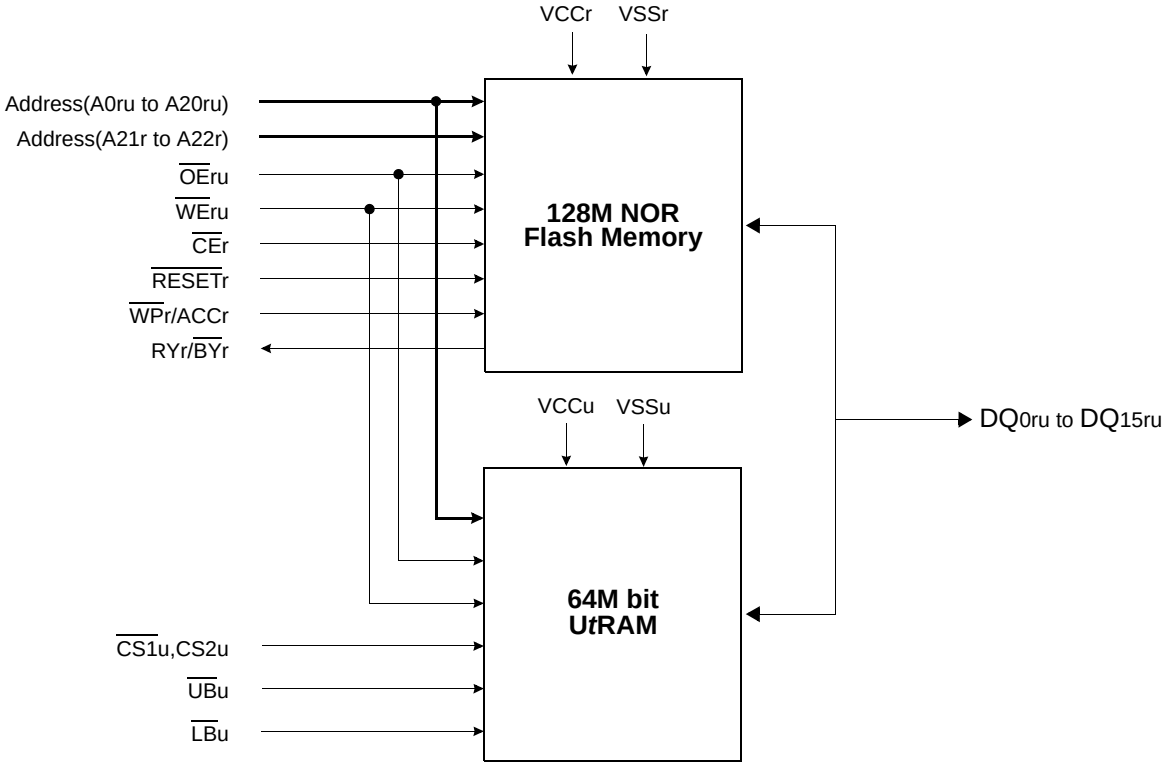
Version
M : 1st Generation

Package
D : FBGA(LF)

Flash Access Time
7 : 70ns

UtRAM Access Time
70 : 70ns

FUNCTIONAL BLOCK DIAGRAM



128M Bit(8Mx16) B-die
Page Mode, Multi Bank NOR Flash

FUNCTIONAL BLOCK DIAGRAM

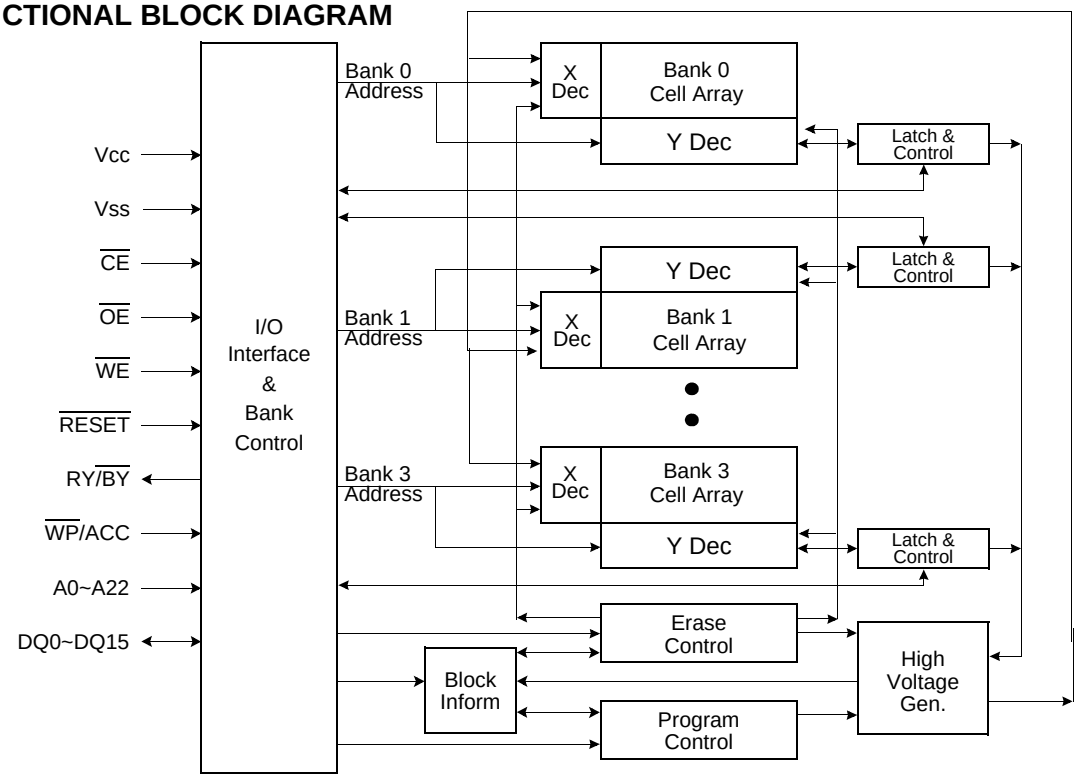


Table 1. PRODUCT LINE-UP

Speed Item	Speed Option			
	4A	4B	4C	4D
Vcc	2.7V~3.6V			
VIO (1)	1.65~1.95V , 2.7~3.6V			
Max. Address Access Time (ns)	55ns	60ns	65ns	70ns
Max. $\overline{CE}$ Access Time (ns)	55ns	60ns	65ns	70ns
Max. $\overline{OE}$ Access Time (ns)	20ns	25ns	25ns	30ns
Max. Page Access Time (ns)	20ns	25ns	25ns	30ns

Notes :
1. Only 4C or 4D speed options can be provided in case of using 1.65~1.95V VIO.

Table 2. DEVICE BANK DIVISIONS

Bank 0, Bank 3		Bank 1, Bank 2	
Mbit	Block Sizes	Mbit	Block Sizes
16 Mbit	4 Kw x 8 and 32 Kw x 31	48 Mbit	32 Kw x 96

Table 3. OTP BLOCK

	Block Address A22~A8	Area	Block Size	Address Range
OTP	0000h	Factory-Locked Area	128 words	000000h-00007Fh
		Customer-Locked Area	128 words	000080h-0000FFh

After entering OTP block, any issued addresses should be in the range of OTP block address

Table 4. DEVICE BANK DIVISIONS

Bank	Number of Blocks	Block Size
0	8	4 Kwords
	31	32 Kwords
1	96	32 Kwords
2	96	32 Kwords
3	31	32 Kwords
	8	4 Kwords

PRODUCT INTRODUCTION

The device is an 128Mbit NOR-type Flash memory. The device features single voltage power supply operating within the range of 2.7V to 3.6V. The device is programmed by using the Channel Hot Electron (CHE) injection mechanism which is used to program EPROMs. The device is erased electrically by using Fowler-Nordheim tunneling mechanism. To provide highly flexible erase and program capability, the device adapts a block memory architecture that divides its memory array into 270 blocks (4 Kw x 16 , 32 Kw x 254). Programming is done in units of 16 bits (Word). All bits of data in one or multiple blocks can be erased simultaneously when the device executes the erase operation. To prevent the device from accidental erasing or over-writing the programmed data, 270 memory blocks can be hardware protected. The device offers fast page access time of 20~30ns with random access time of 55~70ns supporting high speed microprocessors to operate without any wait states.

The command set of device is fully compatible with standard Flash devices. The device is controlled by chip enable ($\overline{CE}$), output enable ($\overline{OE}$) and write enable ($\overline{WE}$). Device operations are executed by selective command codes. The command codes to be combined with addresses and data are sequentially written to the command registers using microprocessor write timing. The command codes serve as inputs to an internal state machine which controls the program/erase circuitry. Register contents also internally latch addresses and data necessary to execute the program and erase operations. The device is implemented with Internal Program/Erase Algorithms to execute the program/erase operations. The Internal Program/Erase Algorithms are invoked by program/erase command sequences. The Internal Program Algorithm automatically programs and verifies data at specified addresses. The Internal Erase Algorithm automatically pre-programs the memory cell which is not programmed and then executes the erase operation. The device has means to indicate the status of completion of program/erase operations. The status can be indicated via the RY/$\overline{BY}$ pin, $\overline{Data}$ polling of DQ7, or the Toggle bit (DQ6). Once the operations have been completed, the device automatically resets itself to the read mode.

Table 5. Operations Table

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{WP}$/ ACC	A9	A6	A1	A0	DQ8/ DQ15	DQ0/ DQ7	$\overline{RESET}$
Read	L	L	H	L/H	A9	A6	A1	A0	D_{OUT}	D_{OUT}	H
Stand-by	Vcc ± 0.2V	X	X	(2)	X	X	X	X	High-Z	High-Z	(2)
Output Disable	L	H	H	L/H	X	X	X	X	High-Z	High-Z	H
Reset	X	X	X	L/H	X	X	X	X	High-Z	High-Z	L
Write	L	H	L	(4)	A9	A6	A1	A0	D_{IN}	D_{IN}	H
Temporary Block Unprotect	X	X	X	(4)	X	X	X	X	X	X	V_{ID}

Notes :

1. L = V_{IL} (Low), H = V_{IH} (High), V_{ID} = 8.5V to 9.5V, D_{IN} = Data in, D_{OUT} = Data out, X = Don't care.
2. $\overline{WP}$/ACC and $\overline{RESET}$ pin are asserted at Vcc±0.2 V or Vss±0.2 V in the Stand-by mode.
3. If $\overline{WP}$/ACC=V_{IL}, the two outermost boot blocks is protected. If $\overline{WP}$/ACC=V_{IH}, the two outermost boot block protection depends on whether those blocks were last protected or unprotected using the method described in "Block Protection and Unprotection". If $\overline{WP}$/ACC=V_{HH}, all blocks will be temporarily unprotected.

COMMAND DEFINITIONS

The device operates by selecting and executing its operational modes. Each operational mode has its own command set. In order to select a certain mode, a proper command with specific address and data sequences must be written into the command register. Writing incorrect information which include address and data or writing an improper command will reset the device to the read mode. The defined valid register command sequences are stated in Table 6. Note that Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Block Erase Operation is in progress. Program Suspend (B0H) and Program Resume (30H) commands are valid during Program Operation and Erase Suspend - Program Operation. Only Read Operation is available after Program Suspend Operation.

Table 6. Command Sequences

Command Sequence		Cycle	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
Read	Addr	1	RA					
	Data		RD					
Reset	Addr	1	XXXH					
	Data		F0H					
Autoselect Manufacturer ID (1,2)	Addr	4	555H	2AAH	DA/555H	DA/X00H		
	Data		AAH	55H	90H	ECH		
Autoselect Device Code (1,2,3)	Addr	4	555H	2AAH	DA/555H	DA/X01H	DA/X0EH	DA/X0FH
	Data		AAH	55H	90H	257EH	2508H	2501H
Autoselect Block Protect Verify (1,2)	Addr	4	555H	2AAH	DA/555H	BA / X02H		
	Data		AAH	55H	90H	(See Table 7)		
Autoselect OTP Factory Protect	Addr	4	555H	2AAH	DA/555H	X03H		
	Data		AAH	55H	90H	(See Note 10)		
Program	Addr	4	555H	2AAH	555H	PA		
	Data		AAH	55H	A0H	PD		
Unlock Bypass	Addr	3	555H	2AAH	555H			
	Data		AAH	55H	20H			
Unlock Bypass Program	Addr	2	XXXH	PA				
	Data		A0H	PD				
Unlock Bypass Block Erase	Addr	2	XXXH	BA				
	Data		80H	30H				
Unlock Bypass Chip Erase	Addr	2	XXXH	XXXH				
	Data		80H	10H				
Unlock Bypass Reset	Addr	2	XXXH	XXXH				
	Data		90H	00H				
Unlock Bypass CFI	Addr	1	XXH					
	Data		98H					
Chip Erase	Addr	6	555H	2AAH	555H	555H	2AAH	555H
	Data		AAH	55H	80H	AAH	55H	10H
Block Erase	Addr	6	555H	2AAH	555H	555H	2AAH	BA
	Data		AAH	55H	80H	AAH	55H	30H
Block Erase Suspend (4, 5)	Addr	1	DA					
	Data		B0H					
Block Erase Resume	Addr	1	DA					
	Data		30H					
Program Suspend (6,7)	Addr	1	DA					
	Data		B0H					
Program Resume	Addr	1	DA					
	Data		30H					
CFI Query (8)	Addr	1	55H					
	Data		98H					

Table 6. Command Sequences (Continued)

Command Definitions		Cycle	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
Accelerated Program	Addr	2	XXH	PA				
	Data		A0H	PD				
Quadruple word Accelerated Program(9)	Addr	5	XXXH	PA1	PA2	PA3	PA4	
	Data		A5H	PD1	PD2	PD3	PD4	
Enter OTP Block Region	Addr	3	555H	2AAH	555H			
	Data		AAH	55H	88H			
Exit OTP Block Region	Addr	4	555H	2AAH	555H	XXX		
	Data		AAH	55H	90H	00H		
OTP Protection bit Program (11,12)	Addr	6	555H	2AAH	555H	OW	OW	OW
	Data		AAH	55H	60H	68H	48H	RD(0)
OTP Protection bit Status	Addr	5	555H	2AAH	555H	OW	OW	
	Data		AAH	55H	60H	48H	RD(0)	

Notes :
- RA : Read Address, PA : Program Address, RD : Read Data, PD : Program Data
- DA : Bank Address (A20- A22), BA : Block Address (A12 - A22), ABP : Address of the block to be protected or unprotected, X = Don't care .
- OW = Address (A7:A0) is (00011010), RD(0) = Read Data DQ0 for protection indicator bit ,RD(1) = Read Data DQ1 for PPB Lock status.
- DQ8 - DQ15 are don't care in command sequence, except for RD and PD.
- A11 - A22 are also don't care, except for the case of special notice.

1. To terminate the Autoselect Mode, it is necessary to write Reset command to the register.
2. The 4th cycle data of Autoselect mode is output data.
   The 3rd and 4th cycle bank addresses of Autoselect mode must be same.
3. Device ID must be read across cycles 4, 5 and 6.
   128Mb(xOEh = 2508h, x0Fh = 2501h), 64Mb(xOEh = 2506h, x0Fh = 2501h),32Mb(xOEh = 2503h, x0Fh = 2501h)
4. The Read / Program operations at non-erasing blocks and the autoselect mode are allowed in the Erase Suspend mode.
5. The Erase Suspend command is applicable only to the Block Erase operation.
6. The Read Operation is allowed in the Program Suspend mode.
7. The Program Suspend command is applicable to Program and Erase Suspend - Program operation.
8. Command is valid when the device is in read mode or Autoselect mode.
9. Quadruple word accelerated program is invoked only at Vpp=Vid, Vpp setup is required prior to this command sequence.
   PA1,PA2,PA3,PA4 have the same A22~A2 address
10. The data is DQ6=1 for customer locked and DQ7=1 for factory locked.
11. Reset command returns device to reading array.
12. Cycle 4 programs the addressed locking bit. Cycle 5 and 6 validate bit has been fully programmed when DQ0=1. If DQ0=0 in cycle 6, program command must be issued and verified again.

Table 7. Autoselect Codes

Description		Address	Read Data
Manufacturer ID		(DA) + 00H	ECH
Device ID	Read Cycle 1	(DA) + 01H	257EH
	Read Cycle 2	(DA) + 0EH	2508H
	Read Cycle 3	(DA) + 0FH	2501H
Block Protection Verification		(BA) + 02H	01H(Proected), 00H (Unproteced)
OTP Indicator Bit (DQ7. DQ6)		(DA) + 03H	DQ7=1(Factory locked), DQ6=1(Customer locked)
Master locking bit Indicator Bit		(BA) + 07H	01H(Proected), 00H (Unproteced)

Notes : 1. L=Logic Low=V_{IL}, H=Logic High=V_{IH}, DA= Bank Address, BA=Block Address, X=Don't care.

DEVICE OPERATION

Read Mode

The device is controlled by Chip Enable ($\overline{CE}$), Output Enable ($\overline{OE}$) and Write Enable ($\overline{WE}$). When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the specified address location,will be the output of the device. The outputs are in high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. The device is available for Page mode. Page mode provides fast access time for high performance system.

Standby Mode

The device features Stand-by Mode to reduce power consumption. This mode puts the device on hold when the device is deselected by making $\overline{CE}$ high ($\overline{CE}$ = V_{IH}). Refer to the DC characteristics for more details on stand-by modes.

Output Disable

The device outputs are disabled when $\overline{OE}$ is High ($\overline{OE}$ = V_{IH}). The output pins are in high impedance state.

Automatic Sleep Mode

The device features Automatic Sleep Mode to minimize the device power consumption. When addresses remain steady for t_{AA}+30ns, the device automatically activates the Automatic Sleep Mode. In the sleep mode, output data is latched and always available to the system. When addresses are changed, the device provides new data without wait time.

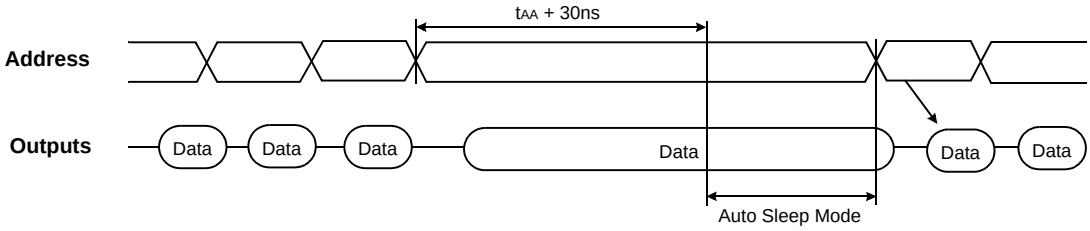
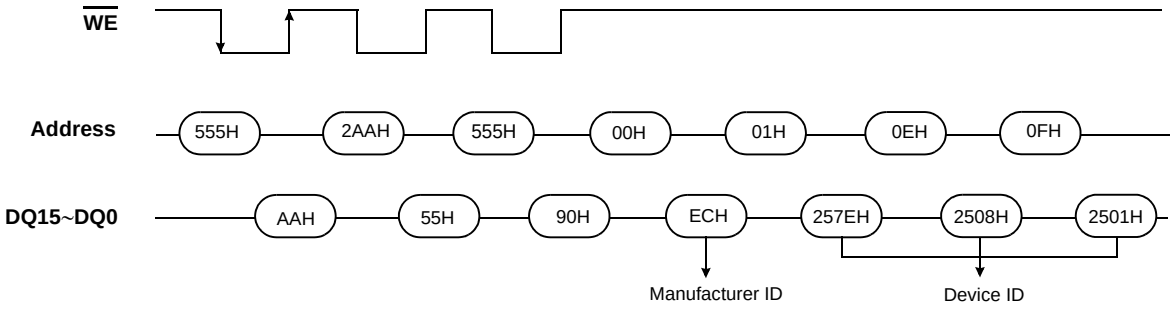


Figure 1. AutoSleep Mode Operation

Autoselect Mode

The device offers the Autoselect Mode to identify manufacturer, device type and block protection verification by reading a binary code. The Autoselect Mode allows programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. In addition, this mode allows the verification of the status of write protected blocks. The manufacturer, device code and block protection verification can be read via the command register. The Command Sequence is shown in Table 6 and Figure 2. The autoselect operation of block protection verification is initiated by first writing two unlock cycle. The third cycle must contain the bank address and autoselect command (90H). To terminate the autoselect operation, write Reset command (F0H) into the command register.



Note : The 3rd Cycle and 4th Cycle address must include the same bank address. Please refer to Table 7 for device code.

Figure 2. Autoselect Operation (by Command Sequence Method)

Write (Program/Erase) Mode

The device executes its program/erase operations by writing commands into the command register. In order to write the commands to the register, $\overline{CE}$ and $\overline{WE}$ must be low and $\overline{OE}$ must be high. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ (whichever occurs last) and the data are latched on the rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever occurs first). The device uses standard microprocessor write timing.

Program

The device can be programmed in units of a word. Programming is writing 0's into the memory array by executing the Internal Program Routine. In order to perform the Internal Program Routine, a four-cycle command sequence is necessary. The first two cycles are unlock cycles. The third cycle is assigned for the program setup command. In the last cycle, the address of the memory location and the data to be programmed at that location are written. The device automatically generates adequate program pulses and verifies the programmed cell margin by the Internal Program Routine. During the execution of the Routine, the system is not required to provide further controls or timings.
During the Internal Program Routine, commands written to the device will be ignored. Note that a hardware reset during a program operation will cause data corruption at the corresponding location.

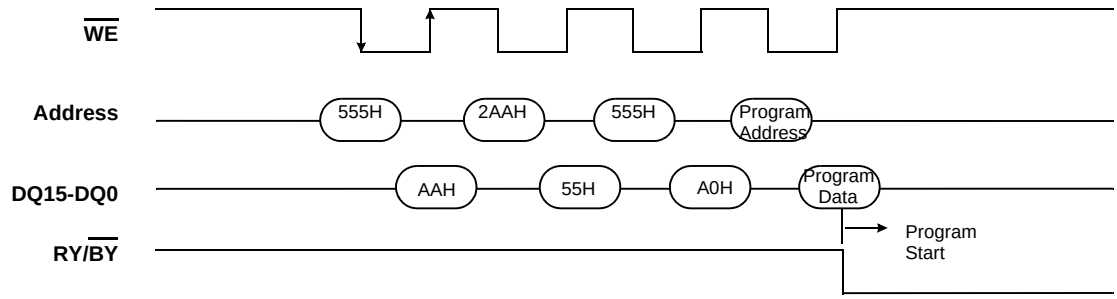


Figure 3. Program Command Sequence

In accross block boundaries and any sequence programming is allowed. A bit cannot be programmed from ’0’ back to ’1’. If attempting to do, it may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still ’0’. Only erase operations can convert a ’0’ to a ’1’.

Unlock Bypass

The device provides the unlock bypass mode to save its operation time. This mode is possible for program, block erase and chip erase operation. There are two methods to enter the unlock bypass mode. The mode is invoked by the unlock bypass command sequence. Unlike the standard program/erase command sequence that contains four to six bus cycles, the unlock bypass program/erase command sequence comprises only two bus cycles. The unlock bypass mode is engaged by issuing the unlock bypass command sequence which is comprised of three bus cycles. Writing first two unlock cycles is followed by a third cycle containing the unlock bypass command (20H). Once the device is in the unlock bypass mode, the unlock bypass program/erase command sequence is necessary. The unlock bypass program command sequence is comprised of only two bus cycles; writing the unlock bypass program command (A0H) is followed by the program address and data. This command sequence is the only valid one for programming the device in the unlock bypass mode. Also, The unlock bypass erase command sequence is comprised of two bus cycles; writing the unlock bypass block erase command(80H-30H) or writing the unlock bypass chip erase command(80H-10H). This command sequences are the only valid ones for erasing the device in the unlock bypass mode. The unlock bypass reset command sequence is the only valid command sequence to exit the unlock bypass mode. The unlock bypass reset command sequence consists of two bus cycles. The first cycle must contain the data (90H). The second cycle contains only the data (00H). Then, the device returns to the read mode.

Chip Erase

To erase a chip is to write 1′s into the entire memory array by executing the Internal Erase Routine. The Chip Erase requires six bus cycles to write the command sequence. The erase set-up command is written after first two "unlock" cycles. Then, there are two more write cycles prior to writing the chip erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory for an all zero data pattern prior to erasing. The automatic erase begins on the rising edge of the last $\overline{WE}$ or $\overline{CE}$ pulse in the command sequence and terminates when DQ7 is "1". After that the device returns to the read mode.

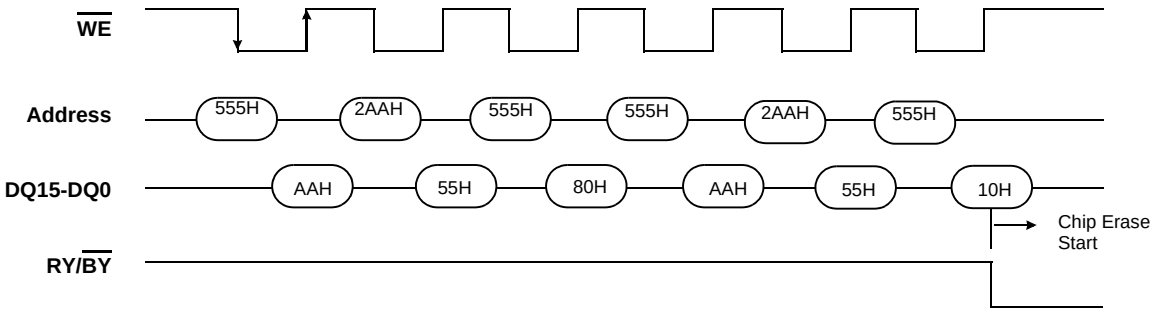


Figure 4. Chip Erase Command Sequence

Block Erase

To erase a block is to write 1′s into the desired memory block by executing the Internal Erase Routine. The Block Erase requires six bus cycles to write the command sequence shown in Table 6. After the first two "unlock" cycles, the erase setup command (80H) is written at the third cycle. Then there are two more "unlock" cycles followed by the Block Erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory prior to erasing it. The block address is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, while the Block Erase command is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$.

Multiple blocks can be erased sequentially by writing the six bus-cycle operation in Figure 6. Upon completion of the last cycle for the Block Erase, additional block address and the Block Erase command (30H) can be written to perform the Multi-Block Erase. An 50us (typical) "time window" is required between the Block Erase command writes. The Block Erase command must be written within the 50us "time window", otherwise the Block Erase command will be ignored. The 50us "time window" is reset when the falling edge of the $\overline{WE}$ occurs within the 50us of "time window" to latch the Block Erase command. During the 50us of "time window", any command other than the Block Erase or the Erase Suspend command written to the device will reset the device to read mode. After the 50 us of "time window", the Block Erase command will initiate the Internal Erase Routine to erase the selected blocks. Any Block Erase address and command following the exceeded "time window" may or may not be accepted. No other commands will be recognized except the Erase Suspend command.

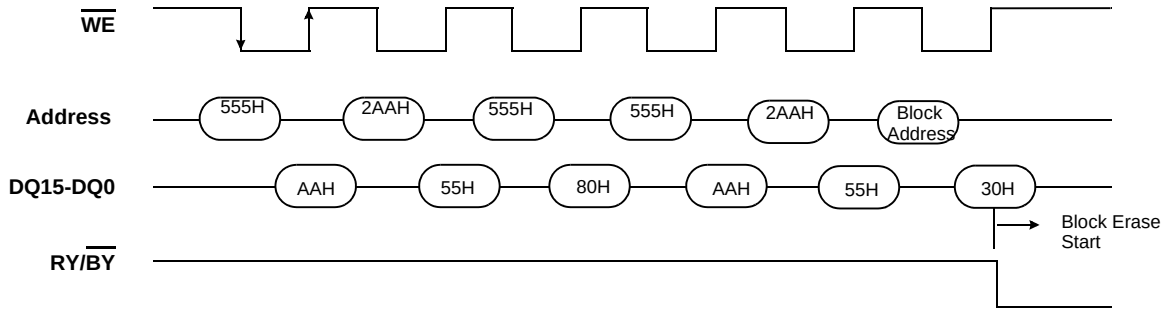


Figure 5. Block Erase Command Sequence

Erase Suspend / Resume

The Erase Suspend command interrupts the Block Erase to read or program data in a block that is not being erased. The Erase Suspend command is only valid during the Block Erase operation including the time window of 50us. The Erase Suspend command is not valid while the Chip Erase or the Internal Program Routine sequence is running.
When the Erase Suspend command is written during a Block Erase operation, the device requires a maximum of 20us to suspend the erase operation. But, when the Erase Suspend command is written during the block erase time window (50us) , the device immediately terminates the block erase time window and suspends the erase operation.
After the erase operation has been suspended, the device is availble for reading or programming data in a block that is not being erased. The system may also write the autoselect command sequence when the device is in the Erase Suspend mode.
When the Erase Resume command is executed, the Block Erase operation will resume. When the Erase Suspend or Erase Resume command is executed, the addresses are in Don't Care state.

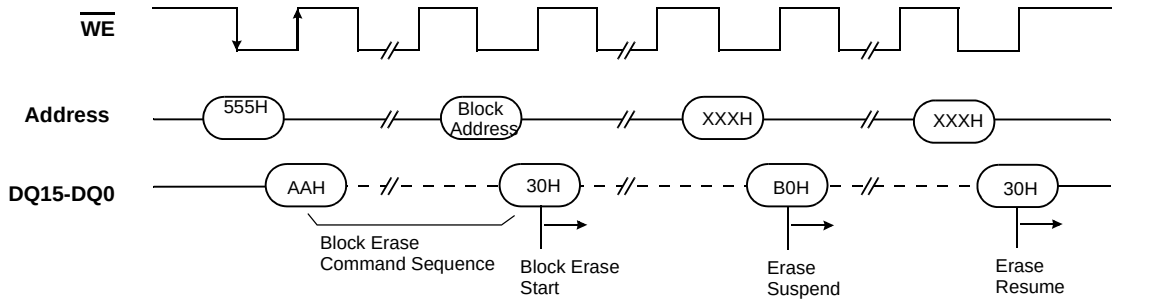


Figure 6. Erase Suspend/Resume Command Sequence

Program Suspend / Resume

The Program Suspend command interrupts the Program operation. Also the Program Suspend command interrupts the Program operation during Erase Suspend Mode. The Read operation is available only during Program Suspend. When the Program Suspend command is written during a Program operation, the device requires a maximum of 10us to suspend the Program operation. The system may also write the autoselect command sequence when the device is in the Program Suspend mode. When the Program Resume command is executed, the Program operation will resume. When the Program Suspend or Program Resume command is executed, the addresses are in Don't Care state.

Read While Write

The device provides multi-bank memory architecture that divides the memory array into four banks. The device is capable of reading data from one bank and writing data to the other bank simultaneously. This is so called the Read While Write operation with multi-bank architecture; this feature provides the capability of executing the read operation during Program/Erase or Erase-Suspend-Program operation. The Read While Write operation is prohibited during the chip erase operation. It is also allowed during erase operation when either single block or multiple blocks from same bank are loaded to be erased. It means that the Read While Write operation is prohibited when blocks from one Bank and another blocks from the other Bank are loaded all together for the multi-block erase operation.

Write Protect ($\overline{WP}$)

The $\overline{WP}$/ACC pin has two useful functions. The one is that certain boot block is protected by the hardware method not to use V_{ID}. The other is that program operation is accelerated to reduce the program time (Refer to Accelerated program Operation Paragraph).
When the $\overline{WP}$/ACC pin is asserted at V_{IL}, the device can not perform program and erase operation in the two "outermost" 4Kword boot blocks on both ends of the flash array independently of whether those blocks were protected or unprotected using the method described in "Block protection/Unprotection". (BA269 and BA268, BA0 and BA1)
The write protected blocks can only be read. This is useful method to preserve an important program data.
When the $\overline{WP}$/ACC pin is asserted at V_{IH}, the device reverts to whether the two outermost 4Kword boot blocks were last set to be protected or unprotected. That is, block protection or unprotection for these two blocks depends on whether they were last protected or unprotected using the method described in "Block protection/unprotection".
Recommend that the $\overline{WP}$/ACC pin must not be in the state of floating or unconnected, otherwise the device may be led to malfunction.

Software Reset

The reset command provides that the bank is reseted to read mode or erase-suspend-read mode. The addresses are in Don't Care state. The reset command is vaild between the sequence cycles in an erase command sequence before erasing begins, or in a program command sequence before programming begins. This resets the bank in which was operating to read mode. if the device is be erasing or programming, the reset command is invalid until the operation is completed. Also, the reset command is valid between the sequence cycles in an autoselect command sequence. In the autoselect mode, the reset command returns the bank to read mode. If a bank entered the autoselect mode in the Erase Suspend mode, the reset command returns the bank to erase-suspend-read mode. If DQ5 is high on erase or program operation, the reset command return the bank to read mode or erase-suspend-read mode if the bank was in the Erase Suspend state.

Hardware Reset

The device offers a reset feature by driving the $\overline{RESET}$ pin to V_{IL}. The $\overline{RESET}$ pin must be kept low (V_{IL}) for at least 500ns. When the $\overline{RESET}$ pin is driven low, any operation in progress will be terminated and the internal state machine will be reset to the standby mode after 20us. If a hardware reset occurs during a program operation, the data at that particular location will be lost. Once the $\overline{RESET}$ pin is taken high, the device requires 200ns of wake-up time until outputs are valid for read access. Also, note that all the data output pins are tri-stated for the duration of the $\overline{RESET}$ pulse.
The $\overline{RESET}$ pin may be tied to the system reset pin. If a system reset occurs during the Internal Program and Erase Routine, the device will be automatically reset to the read mode ; this will enable the systems microprocessor to read the boot-up firmware from the Flash memory.

Power-up Protection

To avoid initiation of a write cycle during Vcc Power-up, $\overline{\text{RESET}}$ low must be asserted during power-up. After $\overline{\text{RESET}}$ goes high, the device is reset to the read mode.

Low Vcc Write Inhibit

To avoid initiation of a write cycle during Vcc power-up and power-down, a write cycle is locked out for Vcc less than 2.3V. If Vcc < V_{LKO} (Lock-Out Voltage), the command register and all internal program/erase circuits are disabled. Under this condition the device will reset itself to the read mode. Subsequent writes will be ignored until the Vcc level is greater than V_{LKO}. It is the user′s responsibility to ensure that the control pins are logically correct to prevent unintentional writes when Vcc is above 2.3V.

Write Pulse Glitch Protection

Noise pulses of less than 5ns(typical) on $\overline{\text{CE}}$, $\overline{\text{OE}}$, or $\overline{\text{WE}}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited under any one of the following conditions : $\overline{\text{OE}}$ = V_{IL}, $\overline{\text{CE}}$ = V_{IH} or $\overline{\text{WE}}$ = V_{IH}. To initiate a write, $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be "0", while $\overline{\text{OE}}$ is "1".

Commom Flash Memory Interface

Common Flash Momory Interface is contrived to increase the compatibility of host system software. It provides the specific information of the device, such as memory size, word configuration, and electrical features. Once this information has been obtained, the system software will know which command sets to use to enable flash writes, block erases, and control the flash component.
When the system writes the CFI command(98H) to address 55H in word mode, the device enters the CFI mode. And then if the system writes the address shown in Table 8, the system can read the CFI data. Query data are always presented on the lowest-order data outputs(DQ0-7) only. In word(x16) mode, the upper data outputs(DQ8-15) is 00h. To terminate this operation, the system must write the reset command.

OTP Block Region

The OTP Block feature provides a 256-word Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The OTP Block is customer lockable and shipped with itself unlocked, allowing customers to untilize the that block in any manner they choose. Indicator bits DQ6 and DQ7 are used to indicate the factory-locked and customer locked status of the part. The data is DQ6 = "1" for customer locked and DQ7 = "1" for factory locked.
The system accesses the OTP Block through a command sequence (see "Enter OTP Block / Exit OTP Block Command sequence" at Table 6). After the system has written the "Enter OTP Block" Command sequence, it may read the OTP Block by using the addresses (000000h~0000FFh) normally and may check the Protection Verify Bit (DQ7,DQ6) by using the "Autoselect Block Protection Verify" Command sequence with OTP Block address. This mode of operation continues until the system issues the "Exit OTP Block" Command suquence, a hardware reset or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to main blocks. Note that the Accelerated function and unlock bypass modes are not available when the OTP Block is enabled.

Customer Lockable
In a Customer lockable device, The OTP Block is one-time programmable and can be locked only once. Note that the Accelerated programming and Unlock bypass functions are not available when programming the OTP Block. Locking operation to the OTP Block is started by writing the "Enter OTP Block" Command sequence, and it can be permanently locked to "1" by issuing the OTP Protection bit program Command sqeunce. Once the OTP block is locked and verified, the system must write the Exit OTP block command to return to reading and writing the remainder of the array.

OTP Protection Bits
OTP protection bits prevent programming of the OTP block memory area. Once set, the OTP area are non-modifiable.

• The OTP Block Lock operation must be used with caution since, once locked, there is no procedure available for unlocking and none of the bits in the OTP Block space can be modified in any way.

• Suspend and resume operation are not supported during OTP protect, nor is OTP protect supported during any suspend operation.

High Voltage Block Protection

Block protection and unprotection may also be implemented using programming equipment. The procedure requires high voltage (Vid) to be placed on the RESET# pin. Refer to Figure 8 for details on this procedure. Note that for block unprotect, all unprotected blocks must first be protected prior to the first sector write cycle.

Accelerated Program Operation

Accelerated program operation reduces the program time through the ACC function. This is one of two functions provided by the $\overline{WP}$/ACC pin. When the $\overline{WP}$/ACC pin is asserted as V_{HH}, the device automatically enters the Unlock Bypass mode, temporarily unprotecting any protected blocks, and reduces the program operation time. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the $\overline{WP}$/ACC pin returns the device to normal operation.

Recommend that the $\overline{WP}$/ACC pin must not be asserted at V_{HH} except on accelerated program operation, or the device may be damaged. In addition, the WP/ACC pin must not be in the state of floating or unconnected, otherwise the device may be led to malfunction.

Single word accelerated program operation

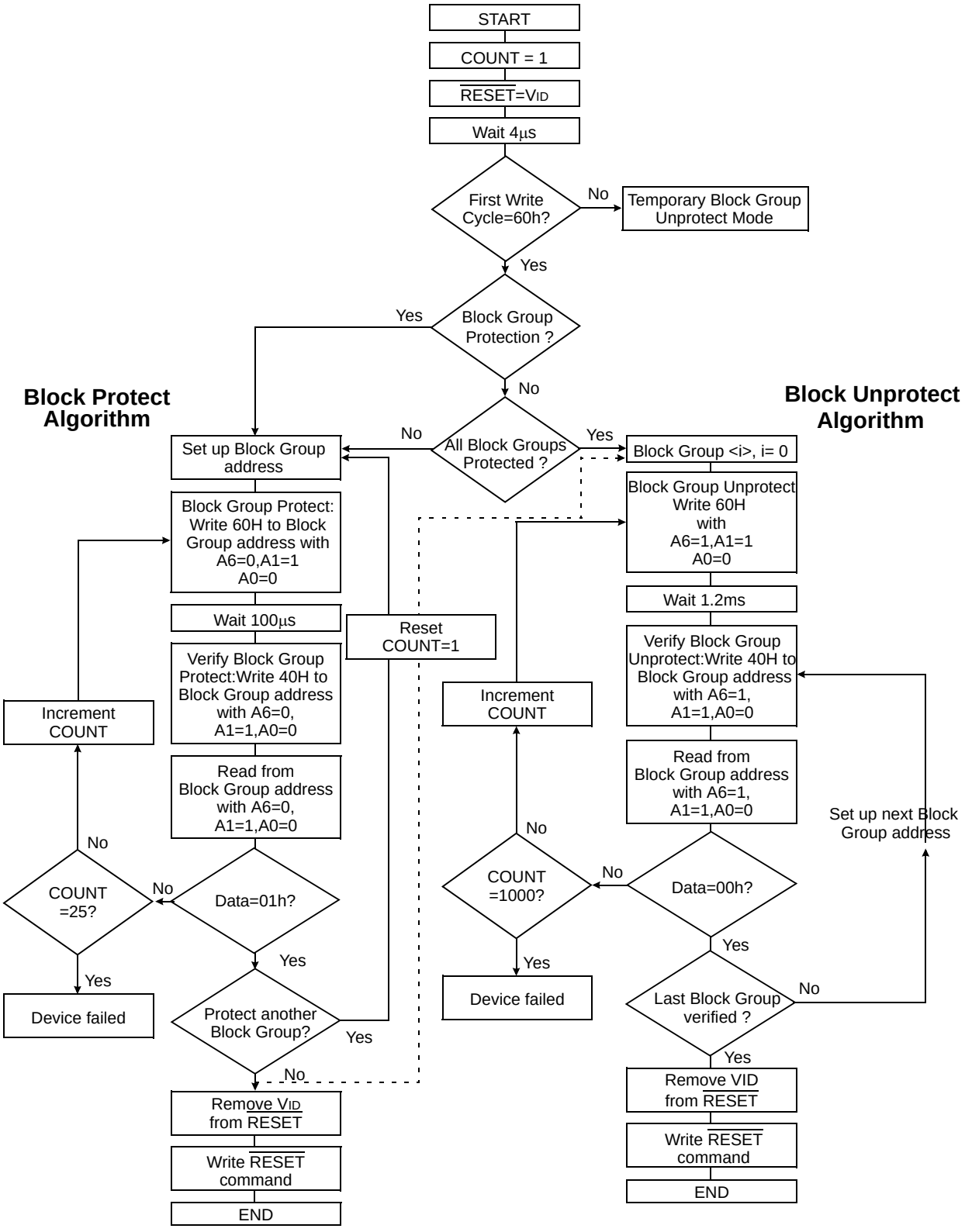
The system would use two-cycle program sequence (One-cycle (XXX - A0H) is for single word program command, and Next one-cycle (PA - PD) is for program address and data).

Quadruple word accelerated program operation

As well as Single word accelerated program, the system would use five-cycle program sequence (One-cycle (XXX - A5H) is for quadruple word program command, and four cycles are for program address and data).

- Only four words programming is possible
- Each program address must have the same A22~A2 address
- The device automatically generates adequate program pulses and ignores other command after program command
- Program/Erase cycling must be limited below 100cycles for optimum performance.
- Read while Write mode is not guaranteed

Requirements : Ambient temperature : T_A=30°C±10°C



Note : All blocks must be protected before unprotect operation is executing.

Figure 7. Block Group Protection & Unprotection Algorithms

Table 8. Block Protection Schemes

DYB	PPB	PPB Lock	Block State
0	0	0	Unprotected-PPB and DYB are changeable
0	0	1	Unprotected-PPB not changeable and DYB are changeable
0	1	0	Protected-PPB and DYB are changeable
1	0	0	
1	1	0	
0	1	1	Protected-PPB not changeable, DYB is changeable
1	0	1	
1	1	1	

Block Protection

The device features several levels of block protection, which can disable both the program and erase operations in certain blocks or block groups:

Persistent Block Protection
A command block protection method that replaces the old 12 V controlled protection method.

Password Block Protection
A highly sophisticated protection method that requires a password before changes to certain blocks or block groups are permitted

Selecting a Block Protection Mode
All parts default to operate in the Persistent Block Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which block protectionmethod will be used. If the Persistent Block Protection method is desired, programming the Persistent Block Protection Mode Locking Bit permanently sets the device to the Persistent Block Protection mode. If the Password Block Protection method is desired, programming the Password Mode Locking Bit permanently sets the device to the Password Block Protection mode.
It is not possible to switch between the two protection modes once a locking bit has been set. One of the two modes must be selected when the device is first programmed. This prevents a program or virus from later setting the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Block Protection Mode into the Password Protection Mode.
The device is shipped with all blocks unprotected. Optional Samsung programming services enable programming and protecting blocks at the factory prior to shipping the device. Contact your local sales office for details.
It is possible to determine whether a block is protected or unprotected. See Autoselect Mode for details.

Persistent Block Protection

The Persistent Block Protection method replaces the 12 V controlled protection method in previous flash devices. This new method provides three different block protection states:
Persistently Locked - The block is protected and cannot be changed.
Dynamically Locked - The block is protected and can be changed by a simple command.
Unlocked - The block is unprotected and can be changed by a simple command.
To achieve these states, three types of "bits" are used:
Persistent Protection Bit
Persistent Protection Bit Lock
Persistent Block Protection Mode Locking Bit

Persistent Protection Bit (PPB)
A single Persistent (non-volatile) Protection Bit is assigned to a maximum four blocks (see the block address tables for specific block protection groupings). All 4 Kword boot-block sectors have individual block Persistent Protection Bits(PPBs) for greater flexibility. Each PPB is individually modifiable through the PPB Write Command.

The device erases all PPBs in parallel. If any PPB requires erasure, the device must be instructed to preprogram all of the block PPBs prior to PPB erasure. Otherwise, a previously erased block PPBs can potentially be over-erased. The flash device does not have a built-in means of preventing block PPBs over-erasure.

Persistent Protection Bit Lock (PPB Lock)
The Persistent Protection Bit Lock (PPB Lock) is a global volatile bit. When set to "1", the PPBs cannot be changed. When cleared "0", the PPBs are changeable. There is only one PPB Lock bit per device. The PPB Lock is cleared after power-up or hardware reset. There is no command sequence to unlock the PPB Lock.

Dynamic Protection Bit (DYB)
A volatile protection bit is assigned for each block. After power-up or hardware reset, the contents of all DYBs is "0". Each DYB is individually modifiable through the DYB Write Command.
When the parts are first shipped, the PPBs are cleared, the DYBs are cleared, and PPB Lock is defaulted to power up in the cleared state - meaning the PPBs are changeable. When the device is first powered on the DYBs power up cleared (blocks not protected). The Protection State for each sector is determined by the logical OR of the PPB and the DYB related to that block. For the blocks that have the PPBs cleared, the DYBs control whether or not the block is protected or unprotected.

By issuing the DYB Write command sequences, the DYBs will be set or cleared, thus placing each block in the protected or unprotected state. These are the so-called Dynamic Locked or Unlocked states. They are called dynamic states because it is very easy to switch back and forth between the protected and unprotected conditions. This allows software to easily protect blocks against inadvertent changes yet does not prevent the easy removal of protection when changes are needed. The DYBs maybe set or cleared as often as needed.

The PPBs allow for a more static, and difficult to change, level of protection. The PPBs retain their state across power cycles because they are non-volatile. Individual PPBs are set with a command but must all be cleared as a group through a complex sequence of program and erasing commands. The PPBs are also limited to 100 erase cycles.

The PPB Lock bit adds an additional level of protection. Once all PPBs are programmed to the desired settings, the PPB Lock may be set to "1". Setting the PPB Lock disables all program and erase commands to the non-volatile PPBs. In effect, the PPB Lock Bit locks the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle. System boot code can determine if any changes to the PPB are needed; for example, to allow new system code to be downloaded. If no changes are needed then the boot code can set the PPB Lock to disable any further changes to the PPBs during system operation.

The WP#/ACC write protect pin adds a final level of hardware protection to blocks BA269 and BA268, BA0 and BA1. When this pin is low it is not possible to change the contents of these blocks. These blocks generally hold system boot code. The WP#/ACC pin can prevent any changes to the boot code that could override the choices made while setting up block protection during system initialization.

For customers who are concerned about malicious viruses there is another level of security - the persistently locked state. To persistently protect a given block or block group, the PPBs associated with that block need to be set to "1". Once all PPBs are programmed to the desired settings, the PPB Lock should be set to "1". Setting the PPB Lock automatically disables all program and erase commands to the Non-Volatile PPBs. In effect, the PPB Lock "freezes" the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle.

It is possible to have blocks that have been persistently locked, and blocks that are left in the dynamic state. The blocks in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DYB Write command sequence is all that is necessary. The DYB write command for the dynamic blocks switch the DYBs to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked blocks, a few more steps are required. First, the PPB Lock bit must be disabled by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB lock bit once again will lock the PPBs, and the device operates normally again.

The best protection is achieved by executing the PPB lock bit set command early in the boot code, and protect the boot code by holding WP#/ACC = VIL.

Table 8 contains all possible combinations of the DYB, PPB, and PPB lock relating to the status of the block.

In summary, if the PPB is set, and the PPB lock is set, the block is protected and the protection can not be removed until the next power cycle clears the PPB lock. If the PPB is cleared, the block can be dynamically locked or unlocked. The DYB then controls whether or not the block is protected or unprotected.

If the user attempts to program or erase a protected block, the device ignores the command and returns to read mode. A program command to a protected block enables status polling for approximately 1us before the device returns to read mode without having modified the contents of the protected block. An erase command to a protected block enables status polling for approximately 50us after which the device returns to read mode without having erased the protected block.

The programming of the DYB, PPB, and PPB lock for a given block can be verified by writing a DYB/PPB/PPB lock verify command to the device.

Persistent Block Protection Mode Locking Bit
Like the password mode locking bit, a Persistent Block Protection mode locking bit exists to guarantee that the device remain in software block protection. Once set, the Persistent Block Protection locking bit prevents programming of the password protection mode locking bit. This guarantees that a hacker could not place the device in password protection mode.

Password Protection Mode

The Password Block Protection Mode method allows an even higher level of security than the Persistent Block Protection Mode. There are two main differences between the Persistent Block Protection and the Password Block Protection Mode:

When the device is first powered on, or comes out of a reset cycle, the PPB Lock bit set to the locked state, rather than cleared to the unlocked state.
The only means to clear the PPB Lock bit is by writing a unique 64-bit Password to the device.
The Password Block Protection method is otherwise identical to the Persistent Block Protection method.
A 64-bit password is the only additional tool utilized in this method.
Once the Password Mode Locking Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear the PPB Lock bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB Lock bit is cleared, and the PPBs can be altered. If they do not match, the flash device does nothing. There is a built-in 2us delay for each "password check." This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

Password and Password Mode Locking Bit
In order to select the Password block protection scheme, the customer must first program the password. The password may be correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Verify operations.

Once the desired password is programmed in, the customer must then set the Password Mode Locking Bit. This operation achieves two objectives:
Permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.
Disables all further commands to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Protection method is desired when setting the Password Mode Locking Bit. More importantly, the user must be sure that the password is correct when the Password Mode Locking Bit is set. Due to the fact that read operations are disabled, there is no means to verify what the password is afterwards. If the password is lost after setting the Password Mode Locking Bit, there will be no way to clear the PPB Lock bit.

The Password Mode Locking Bit, once set, prevents reading the 64-bit password on the DQ bus and further password programming. The Password Mode Locking Bit is not erasable. Once Password Mode Locking Bit is programmed, the Persistent Block Protection Locking Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

64-bit Password
The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Verify commands (see "Password Verify Command"). The password function works in conjunction with the Password Mode Locking Bit, which when set, prevents the Password Verify command from reading the contents of the password on the pins of the device.

Write Protect (WP#)
The Write Protect feature provides a hardware method of protecting the upper two and lower two blocks without using VID. This function is provided by the WP# pin and overrides the previously discussed "High Voltage Block Protection" section method.

If the system asserts VIL on the WP#/ACC pin, the device disables program and erase functions in the two outermost 4 Kword blocks on both ends of the flash array independent of whether it was previously protected or unprotected.

If the system asserts VIH on the WP#/ACC pin, the device reverts the upper two and lower two blocks to whether they were last set to be protected or unprotected. That is, block protection or unprotection for these sectors depends on whether they were last protected or unprotected using the method described in the "High Voltage Block Protection" section.

Persistent Protection Bit Lock

The Persistent Protection Bit (PPB) Lock is a volatile bit that reflects the state of the Password Mode Locking Bit after power-up reset. If the Password Mode Lock Bit is also set after a hardware reset (RESET# asserted) or a power-up reset, the ONLY means for clearing the PPB Lock Bit in Password Protection Mode is to issue the Password Unlock command. Successful execution of the Password Unlock command clears the PPB Lock Bit, allowing for block PPBs modifications. Asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit to a "1" when the Password Mode Lock Bit is not set.

If the Password Mode Locking Bit is not set, including Persistent Protection Mode, the PPB Lock Bit is cleared after power-up or hardware reset. The PPB Lock Bit is set by issuing the PPB Lock Bit Set command. Once set the only means for clearing the PPB Lock Bit is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Protection Mode.

Master locking bit set

This Master locking bit can ensure that protected blocks be permanently unalterable.
Master locking bit is non-volatile bit. Master locking bit controls protection status of entire blocks.
The usage of the master locking bit command sequence is absolutely required to ensure full protection of data from future alterations. If master locking bit is set ("1"), entire blocks are permanently protected. They are not changed and altered by any future lock/unlock commands.
Anyone who uses this fuction needs much attention. Because there is no way to return to unlock status. Default status of master locking bit is unlock status("0").
If Master locking bit sets on unprotected block, the block still are remaining in status of unprotected block.
The unprotected block can be protected by protection command.

Table 9. Boot Block/Block Addresses for Protection / Unprotection

Block	A22-A12	Block Size
BA0	00000000000	4 Kwords
BA1	00000000001	4 Kwords
BA2	00000000010	4 Kwords
BA3	00000000011	4 Kwords
BA4	00000000100	4 Kwords
BA5	00000000101	4 Kwords
BA6	00000000110	4 Kwords
BA7	00000000111	4 Kwords
BA8	00000001XXX	32 Kwords
BA9	00000010XXX	32 Kwords
BA10	00000011XXX	32 Kwords
BA11-BA14	000001XXXXX	128 (4x32) Kwords
BA15-BA18	000010XXXXX	128 (4x32) Kwords
BA19-BA22	000011XXXXX	128 (4x32) Kwords
BA23-BA26	000100XXXXX	128 (4x32) Kwords
BA27-BA30	000101XXXXX	128 (4x32) Kwords
BA31-BA34	000110XXXXX	128 (4x32) Kwords
BA35-BA38	000111XXXXX	128 (4x32) Kwords
BA39-BA42	001000XXXXX	128 (4x32) Kwords
BA43-BA46	001001XXXXX	128 (4x32) Kwords
BA51-BA54	001010XXXXX	128 (4x32) Kwords
BA55-BA58	001011XXXXX	128 (4x32) Kwords
BA59-BA62	001101XXXXX	128 (4x32) Kwords
BA63-BA66	001110XXXXX	128 (4x32) Kwords
BA67-BA70	001111XXXXX	128 (4x32) Kwords
BA71-BA74	010000XXXXX	128 (4x32) Kwords
BA75-BA78	010001XXXXX	128 (4x32) Kwords
BA79-BA82	010010XXXXX	128 (4x32) Kwords
BA83-BA86	010011XXXXX	128 (4x32) Kwords
BA87-BA90	010100XXXXX	128 (4x32) Kwords
BA91-BA94	010101XXXXX	128 (4x32) Kwords
BA95-BA98	010110XXXXX	128 (4x32) Kwords
BA99-BA102	010111XXXXX	128 (4x32) Kwords
BA103-BA106	011000XXXXX	128 (4x32) Kwords
BA107-BA110	011001XXXXX	128 (4x32) Kwords
BA111-BA114	011010XXXXX	128 (4x32) Kwords
BA115-BA118	011011XXXXX	128 (4x32) Kwords
BA119-BA122	011100XXXXX	128 (4x32) Kwords
BA123-BA126	011101XXXXX	128 (4x32) Kwords
BA127-BA130	011110XXXXX	128 (4x32) Kwords
BA131-BA134	011111XXXXX	128 (4x32) Kwords
BA135-BA138	100000XXXXX	128 (4x32) Kwords
BA139-BA142	100001XXXXX	128 (4x32) Kwords
BA143-BA146	100010XXXXX	128 (4x32) Kwords
BA147-BA150	100011XXXXX	128 (4x32) Kwords

Table 9. Boot Block/Block Addresses for Protection / Unprotection (Continued)

Block	A22-A12	Block Size
BA151-BA154	100100XXXXX	128 (4x32) Kwords
BA155-BA158	100101XXXXX	128 (4x32) Kwords
BA159-BA162	100110XXXXX	128 (4x32) Kwords
BA163-BA166	100111XXXXX	128 (4x32) Kwords
BA167-BA170	101000XXXXX	128 (4x32) Kwords
BA171-BA174	101001XXXXX	128 (4x32) Kwords
BA175-BA178	101010XXXXX	128 (4x32) Kwords
BA179-BA182	101011XXXXX	128 (4x32) Kwords
BA183-BA186	101100XXXXX	128 (4x32) Kwords
BA187-BA190	101101XXXXX	128 (4x32) Kwords
BA191-BA194	101110XXXXX	128 (4x32) Kwords
BA195-BA198	101111XXXXX	128 (4x32) Kwords
BA199-BA202	110000XXXXX	128 (4x32) Kwords
BA203-BA206	110001XXXXX	128 (4x32) Kwords
BA207-BA210	110010XXXXX	128 (4x32) Kwords
BA211-BA214	110011XXXXX	128 (4x32) Kwords
BA215-BA218	110100XXXXX	128 (4x32) Kwords
BA219-BA222	110101XXXXX	128 (4x32) Kwords
BA223-BA226	110110XXXXX	128 (4x32) Kwords
BA227-BA230	110111XXXXX	128 (4x32) Kwords
BA231-BA234	111000XXXXX	128 (4x32) Kwords
BA235-BA238	111001XXXXX	128 (4x32) Kwords
BA239-BA242	111010XXXXX	128 (4x32) Kwords
BA243-BA246	111011XXXXX	128 (4x32) Kwords
BA247-BA250	111100XXXXX	128 (4x32) Kwords
BA251-BA254	111101XXXXX	128 (4x32) Kwords
BA255-BA258	111110XXXXX	128 (4x32) Kwords
BA259	11111100XXX	32 Kwords
BA260	11111101XXX	32 Kwords
BA261	11111110XXX	32 Kwords
BA262	11111111000	4 Kwords
BA263	11111111001	4 Kwords
BA264	11111111010	4 Kwords
BA265	11111111011	4 Kwords

Table 10. Block Protection Command Sequences

Command Sequence		Cycle	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle	7th Cycle
Password Program(1,2)	Addr	4	555H	2AAH	555H	XX[0-3]H			
	Data		AAH	55H	38H	PD[0-3]			
Password Verify(2,4,5)	Addr	4	555H	2AAH	555H	PWA[0-3]			
	Data		AAH	55H	C8H	PWD[0-3]			
Password Unlock(3,6,7)	Addr	7	555H	2AAH	555H	PWA[0]	PWA[1]	PWA[2]	PWA[3]
	Data		AAH	55H	28H	PWD[0]	PWD[1]	PWD[2]	PWD[3]
PPB Program(1,2,8)	Addr	6	555H	2AAH	555H	(BA)WP	(BA)WP	(BA)WP	
	Data		AAH	55H	60H	68H	48H	RD(0)	
Master locking bit Set	Addr	3	555H	2AAH	555H				
	Data		AAH	55H	F1H				
PPB Status	Addr	4	555H	2AAH	555H	(BA)WP			
	Data		AAH	55H	90H	RD(0)			
All PPB Erase(1,2,9,10)	Addr	6	555H	2AAH	555H	WP	(BA)	(BA)WP	
	Data		AAH	55H	60H	60H	40H	RD(0)	
PPB Lock Bit Set	Addr	3	555H	2AAH	555H				
	Data		AAH	55H	78H				
PPB Lock Bit Status(11)	Addr	4	555H	2AAH	555H	BA			
	Data		AAH	55H	58H	RD(1)			
DYB Write(3)	Addr	4	555H	2AAH	555H	BA			
	Data		AAH	55H	48H	X1H			
DYB Erase(3)	Addr	4	555H	2AAH	555H	BA			
	Data		AAH	55H	48H	X0H			
DYB Status(2)	Addr	4	555H	2AAH	(DA)555H	BA			
	Data		AAH	55H	58H	RD(0)			
PPMLB Program(1,2,8)	Addr	6	555H	2AAH	555H	PL	PL	PL	
	Data		AAH	55H	60H	68H	48H	RD(0)	
PPMLB Status(1)	Addr	5	555H	2AAH	555H	PL	PL		
	Data		AAH	55H	60H	48H	RD(0)		
SPMLB Program(1,2,8)	Addr	6	555H	2AAH	555H	BL	BL	BL	
	Data		AAH	55H	60H	68	48	RD(0)	
SPMLB Status(1)	Addr	5	555H	2AAH	555H	BL	BL		
	Data		AAH	55H	60H	48	RD(0)		

Legend:

DYB = Dynamic Protection Bit
OW = Address (A7:A0) is (00011010)
PD[3:0] = Password Data (1 of 4 portions)
PPB = Persistent Protection Bit
PWA = Password Address. A1:A0 selects portion of password.
PWD = Password Data being verified.
PL = Password Protection Mode Lock Address (A7:A0) is (00001010)
RD(0) = Read Data DQ0 for protection indicator bit.
RD(1) = Read Data DQ1 for PPB Lock status.
BA = Block Address where security command applies. Address bits Amax:A12 uniquely select any block.
BL = Persistent Protection Mode Lock Address (A7:A0) is (00010010)
WP = PPB Address (A7:A0) is (00000010)
X = Don't care
PPMLB = Password Protection Mode Locking Bit
SPMLB = Persistent Protection Mode Locking Bit

Notes:
- See the description of bus operations.
- All values are in hexadecimal.
- Shaded cells in table denote read cycles. All other cycles are write operations.
- During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.

1. The reset command returns device to reading array.
2. Cycle 4 programs the addressed locking bit. Cycles 5 and 6 validate bit has been fully programmed when DQ0 = 1. If DQ0 = 0 in cycle 6, program command must be issued and verified again.
3. Data is latched on the rising edge of WE#.
4. Entire command sequence must be entered for each portion of password.
5. Command sequence returns FFh if PPMLB is set.
6. The password is written over four consecutive cycles, at addresses 0-3.
7. A 2us timeout is required between any two portions of password.
8. A 100us timeout is required between cycles 4 and 5.
9. A 1.2 ms timeout is required between cycles 4 and 5.
10. Cycle 4 erases all PPBs. Cycles 5 and 6 validate bits have been fully erased when DQ0 = 0. If DQ0 = 1 in cycle 6, erase command must be issued and verified again. Before issuing erase command, all PPBs should be programmed to prevent PPB overerasure.
11. DQ1 = 1 if PPB locked, 0 if unlocked.

Table 11. Common Flash Memory Interface Code

Description	Addresses (Word Mode)	Data
Query Unique ASCII string "QRY"	10H 11H 12H	0051H 0052H 0059H
Primary OEM Command Set	13H 14H	0002H 0000H
Address for Primary Extended Table	15H 16H	0040H 0000H
Alternate OEM Command Set (00h = none exists)	17H 18H	0000H 0000H
Address for Alternate OEM Extended Table (00h = none exists)	19H 1AH	0000H 0000H
Vcc Min. (write/erase) D7-D4: volt, D3-D0: 100 millivolt	1BH	0027H
Vcc Max. (write/erase) D7-D4: volt, D3-D0: 100 millivolt	1CH	0036H
Vpp Min. voltage(00H = no Vpp pin present)	1DH	0000H
Vpp Max. voltage(00H = no Vpp pin present)	1EH	0000H
Typical timeout per single word write 2^N us	1FH	0003H
Typical timeout for Min. size buffer write 2^N us(00H = not supported)	20H	0000H
Typical timeout per individual block erase 2^N ms	21H	0009H
Typical timeout for full chip erase 2^N ms(00H = not supported)	22H	0000H
Max. timeout for word write 2^N times typical	23H	0004H
Max. timeout for buffer write 2^N times typical	24H	0000H
Max. timeout per individual block erase 2^N times typical	25H	0004H
Max. timeout for full chip erase 2^N times typical(00H = not supported)	26H	0000H
Device Size = 2^N byte	27H	0018H
Flash Device Interface description	28H 29H	0001H 0000H
Max. number of byte in multi-byte write = 2^N	2AH 2BH	0000H 0000H
Number of Erase Block Regions within device	2CH	0003H
Erase Block Region 1 Information	2DH 2EH 2FH 30H	0007H 0000H 0020H 0000H
Erase Block Region 2 Information	31H 32H 33H 34H	00FDH 0000H 0000H 0001H
Erase Block Region 3 Information	35H 36H 37H 38H	0007H 0000H 0020H 0000H
Erase Block Region 4 Information	39H 3AH 3BH 3CH	0000H 0000H 0000H 0000H

Table 11. Common Flash Memory Interface Code

Description	Addresses (Word Mode)	Data
Query-unique ASCII string "PRI"	40H 41H 42H	0050H 0052H 0049H
Major version number, ASCII	43H	0030H
Minor version number, ASCII	44H	0030H
Address Sensitive Unlock(Bits 1-0) 0 = Required, 1= Not Required Silcon Revision Number(Bits 7-2)	45H	0000H
Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write	46H	0002H
Block Protect 00 = Not Supported, 01 = Supported	47H	0001H
Block Temporary Unprotect 00 = Not Supported, 01 = Supported	48H	0001H
Block Protect/Unprotect scheme, 00 = Not Supported, 01 = Supported	49H	0001H
Simultaneous Operation 00 = Not Supported, 01 = Supported	4AH	0001H
Burst Mode Type 00 = Not Supported, 01 = Supported	4BH	0000H
Page Mode Type 00 = Not Supported, 01 = 4 Word Page 02 = 8 Word Page	4CH	0002H
ACC(Acceleration) Supply Minimum 00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV	4DH	0085H
ACC(Acceleration) Supply Maximum 00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV	4EH	0095H
Top/Bottom Boot Block Flag 02H = Bottom Boot Device, 03H = Top Boot Device, 04H = Top and Bottom Device	4FH	0004H

DEVICE STATUS FLAGS

The device has means to indicate its status of operation in the bank where a program or erase operation is in processes. Address must include bank address being excuted internal routine operation. The status is indicated by raising the device status flag via corresponding DQ pins or the RY/ $\overline{BY}$ pin. The corresponding DQ pins are DQ7, DQ6, DQ5, DQ3 and DQ2. The statuses are as follows :

Table 12. Hardware Sequence Flags

	Status		DQ7	DQ6	DQ5	DQ3	DQ2	RY/$\overline{BY}$
In Progress	Programming		$\overline{DQ7}$	Toggle	0	0	1	0
	Block Erase or Chip Erase		0	Toggle	0	1	Toggle	0
	Erase Suspend Read	Erase Suspended Block	1	1	0	0	Toggle (Note 1)	1
	Erase Suspend Read	Non-Erase Suspended Block	Data	Data	Data	Data	Data	1
	Erase Suspend Program	Non-Erase Suspended Block	$\overline{DQ7}$	Toggle	0	0	1	0
	Program Suspend Read	Program Suspended Block	DQ7	1	0	0	Toggle (Note 1)	1
	Program Suspend Read	Non-Program Suspended Block	Data	Data	Data	Data	Data	1
Exceeded Time Limits	Programming		$\overline{DQ7}$	Toggle	1	0	No Toggle	0
	Block Erase or Chip Erase		0	Toggle	1	1	(Note 2)	0
	Erase Suspend Program		$\overline{DQ7}$	Toggle	1	0	No Toggle	0

Notes :
1. DQ2 will toggle when the device performs successive read operations from the erase/program suspended block.
2. If DQ5 is High (exceeded timing limits), successive reads from a problem block will cause DQ2 to toggle.

DQ7 : $\overline{\text{Data}}$ Polling

When an attempt to read the device is made while executing the Internal Program, the complement of the data is written to DQ7 as an indication of the Routine in progress. When the Routine is completed an attempt to access to the device will produce the true data written to DQ7. When a user attempts to read the block being erased, DQ7 will be low. If the device is placed in the Erase/Program Suspend Mode, the status can be detected via the DQ7 pin. If the system tries to read an address which belongs to a block that is being erase suspended, DQ7 will be high. And, if the system tries to read an address which belongs to a block that is being program suspended, the output will be the true data of DQ7 itself. If a non-erase-suspended or non-program-suspended block address is read, the device will produce the true data to DQ7. If an attempt is made to program a protected block, DQ7 outputs complements the data for approximately 1μs and the device then returns to the Read Mode without changing data in the block. If an attempt is made to erase a protected block, DQ7 outputs complement data in approximately 100us and the device then returns to the Read Mode without erasing the data in the block.

DQ6 : Toggle Bit

Toggle bit is another option to detect whether an Internal Routine is in progress or completed. Once the device is at a busy state, DQ6 will toggle. Toggling DQ6 will stop after the device completes its Internal Routine. If the device is in the Erase/Program Suspend Mode, an attempt to read an address that belongs to a block that is being erased or programmed will produce a high output of DQ6. If an address belongs to a block that is not being erased or programmed, toggling is halted and valid data is produced at DQ6. If an attempt is made to program a protected block, DQ6 toggles for approximately 1us and the device then returns to the Read Mode without changing the data in the block. If an attempt is made to erase a protected block, DQ6 toggles for approximately 100μs and the device then returns to the Read Mode without erasing the data in the block.

DQ5 : Exceed Timing Limits

If the Internal Program/Erase Routine extends beyond the timing limits, DQ5 will go High, indicating program/erase failure.

DQ3 : Block Erase Timer

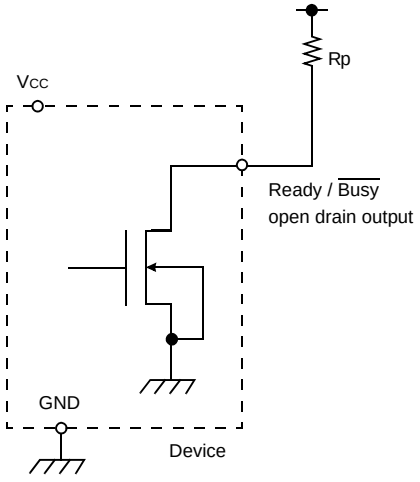
The status of the multi-block erase operation can be detected via the DQ3 pin. DQ3 will go High if 50μs of the block erase time window expires. In this case, the Internal Erase Routine will initiate the erase operation.Therefore, the device will not accept further write commands until the erase operation is completed. DQ3 is Low if the block erase time window is not expired. Within the block erase time window, an additional block erase command (30H) can be accepted. To confirm that the block erase command has been accepted, the software may check the status of DQ3 following each block erase command.

DQ2 : Toggle Bit 2

The device generates a toggling pulse in DQ2 only if an Internal Erase Routine or an Erase/Program Suspend is in progress. When the device executes the Internal Erase Routine, DQ2 toggles only if an erasing bank is read. Although the Internal Erase Routine is in the Exceeded Time Limits, DQ2 toggles only if an erasing block in the Exceeded Time Limits is read. When the device is in the Erase/Program Suspend mode, DQ2 toggles only if an address in the erasing or programming block is read. If a non-erasing or non-programmed block address is read during the Erase/Program Suspend mode, then DQ2 will produce valid data. DQ2 will go High if the user tries to program a non-erase suspend block while the device is in the Erase Suspend mode.

RY/$\overline{BY}$: Ready/$\overline{Busy}$

The device has a Ready / $\overline{Busy}$ output that indicates either the completion of an operation or the status of Internal Algorithms. If the output is Low, the device is busy with either a program or an erase operation. If the output is High, the device is ready to accept any read/write or erase operation. When the RY/ $\overline{BY}$ pin is low, the device will not accept any additional program or erase commands with the exception of the Erase Suspend command. If the device is placed in an Erase Suspend mode, the RY/ $\overline{BY}$ output will be High. For programming, the RY/ $\overline{BY}$ is valid (RY/ $\overline{BY}$ = 0) after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence. For Chip Erase, RY/ $\overline{BY}$ is also valid after the rising edge of $\overline{WE}$ pulse in the six write pulse sequence. For Block Erase, RY/ $\overline{BY}$ is also valid after the rising edge of the sixth $\overline{WE}$ pulse.
The pin is an open drain output, allowing two or more Ready/ $\overline{Busy}$ outputs to be OR-tied. An appropriate pull-up resistor is required for proper operation.



$$Rp = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2\ V}{2.1mA + \Sigma I_L}$$

where ΣI_L is the sum of the input currents of all devices tied to the Ready / $\overline{Busy}$ pin.

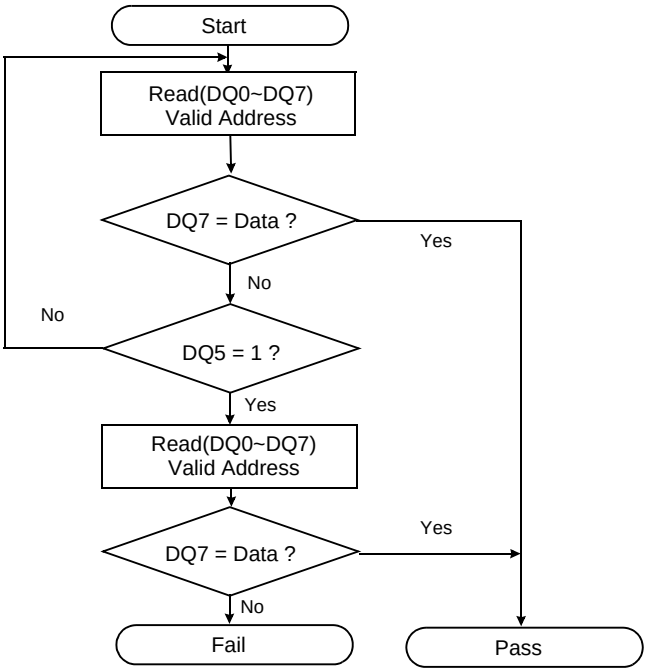


Figure 8. Data Polling Algorithms

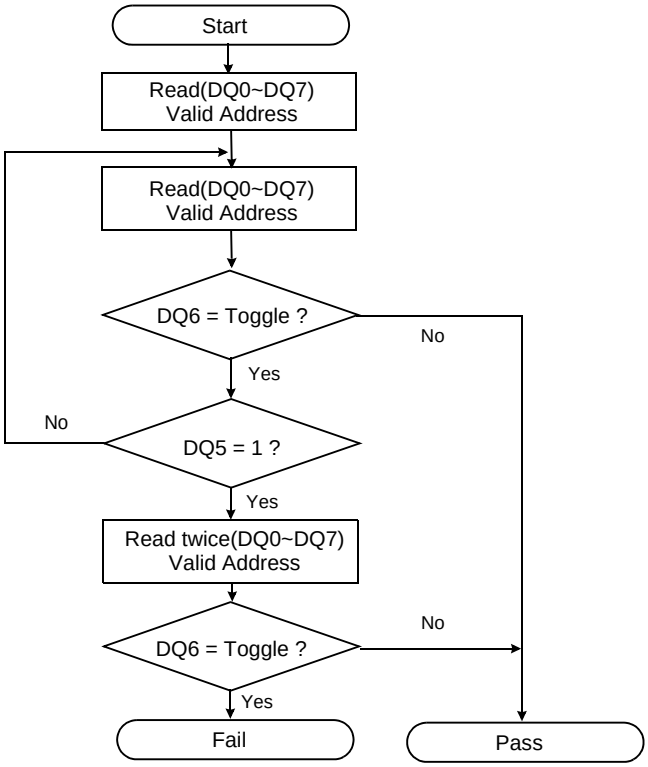


Figure 9. Toggle Bit Algorithms

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	Vcc	Vcc	-0.5 to +4.0	V
	A9, $\overline{OE}$, $\overline{RESET}$	V_{IN}	-0.5 to +9.5	
	$\overline{WP}$/ACC		-0.5 to +9.5	
	All Other Pins		-0.5 to +2.5	
Temperature Under Bias		T_{bias}	-25 to +125	°C
Storage Temperature		T_{stg}	-65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA
Operating Temperature		T_A	-25 to + 85	°C

Notes :

1. Minimum DC voltage is -0.5V on Input/ Output pins. During transitions, this level may fall to -2.0V for periods <20ns. Maximum DC voltage on input / output pins is Vcc+0.5V which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.
2. Minimum DC voltage is -0.5V on A9, $\overline{OE}$, $\overline{RESET}$ and $\overline{WP}$/ACC pins. During transitions, this level may fall to -2.0V for periods <20ns. Maximum DC voltage on A9, $\overline{OE}$, $\overline{RESET}$, $\overline{WP}$/ACC pins is 9.5V which, during transitions, may overshoot to 14.0V for periods <20ns.
3. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to GND)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc	2.7	3.0	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Sym-bol	Test Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	VIN=VSS to VCC, VCC=VCCmax		– 1.0	-	+ 1.0	μA
A9,$\overline{OE}$,$\overline{RESET}$ Input Leakage Current	I_{LIT}	VCC=VCCmax, A9,$\overline{OE}$,$\overline{RESET}$=9.5V		-	-	35	μA
$\overline{WP}$/ACC Input Leakage Current	I_{LIW}	VCC=VCCmax, $\overline{WP}$/ACC=9.5V		-	-	35	μA
Output Leakage Current	I_{LO}	VOUT=VSS to VCC,VCC=VCC-max,$\overline{OE}$=VIH		– 1.0	-	+ 1.0	μA
Active Read Current (1)	I_{CC1}	$\overline{OE}$=VIH, VCC=VCCmax	10MHz	-	45	55	mA
			5MHz	-	20	30	
Active Write Current (2)	I_{CC2}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}, $\overline{WE}$=V_{IL}		-	15	30	mA
Read While Program Current (3)	I_{CC3}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH} (@10Mhz)		-	35	55	mA
Read While Erase Current (3)	I_{CC4}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH} (@10Mhz)		-	35	55	mA
Program While Erase Suspend Current	I_{CC5}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}		-	15	35	mA
Page Read Current	I_{CC6}	$\overline{OE}$=V_{IH}, 8 word Page Read		-	10	15	mA
ACC Accelerated Program Current	I_{ACC}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}		-	15	30	mA
Standby Current	I_{SB1}	$\overline{CE}$, $\overline{RESET}$, $\overline{WP}$/ACC= V_{IO}± 0.3		-	15	30	μA
Standby Current During Reset	I_{SB2}	$\overline{RESET}$= Vss± 0.3		-	15	30	μA
Automatic Sleep Mode	I_{SB3}	V_{IH}=V_{IO} ± 0.3V, V_{IL}=V_{SS} ±0.2V		-	15	30	μA
Input Low Level	V_{IL}	Vio=1.65~1.95V(2.7~3.6V)		-0.4(-0.5)	-	0.4(0.8)	V
Input High Level	V_{IH}	Vio=1.65~1.95V(2.7~3.6V)		Vio-0.4(2.0)	-	Vio+0.4(Vcc+0.3)	V
Voltage for $\overline{WP}$/ACC Block Temporarily Unprotect and Program Acceleration (4)	V_{HH}	Vcc = 3.0V ± 0.15V		8.5	-	9.5	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Voltage for Autoselect and Block Protect (4)	V_{ID}	V_{CC} = 3.0V ± 10%	8.5	-	9.5	V
Output Low Level	V_{OL}	IOL =100uA,Vcc=VCCmin, Vio=1.65~1.95V	-		0.1	V
		IOL =2.0mA,Vcc=VCCmin, Vio=2.7~3.6V	-		0.4	V
Output High Level	V_{OH}	IOH = -100uA, Vcc=VCCmin, Vio=1.65~1.95V	Vio-0.1	-	-	V
		IOH = -2.0mA, Vcc=VCCmin, Vio=2.7~3.6V	2.4	-	-	V
Low VCC Lock-out Voltage (5)	V_{LKO}		2.3	-	2.5	V

Notes :
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component(at 10 MHz).
2. I_{CC} active during Internal Routine(program or erase) is in progress.
3. I_{CC} active during Read while Write is in progress.
4. The high voltage (V_{HH} or V_{ID}) must be used in the range of Vcc = 3.0V ± 0.15V
5. Not 100% tested.
6. Typical value are measured at Vcc = 3.0V,T_A=25°C , Not 100% tested.

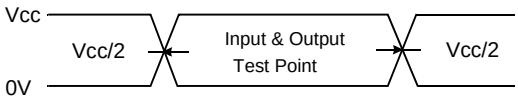
CAPACITANCE(T_A = 25 °C, V_{CC} = 3.0V, f = 1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	10	pF
Control Pin Capacitance	C_{IN2}	V_{IN}=0V	-	10	pF

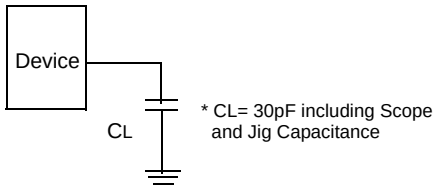
Note : Capacitance is periodically sampled and not 100% tested.

AC TEST CONDITION

Parameter	Value
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times(Vio=1.8,3.0V)	5ns
Input and Output Timing Levels	Vcc/2
Output Load	C_L = 30pF



Input Pulse and Test Point



Output Load

AC CHARACTERISTICS
Read Operations

Parameter	Symbol	Vcc=2.7V~3.6V								Unit
		4A		4B		4C		4D		
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time (1)	t_{RC}	55	-	60	-	65	-	70	-	ns
Address Access Time	t_{AA}	-	55	-	60	-	65	-	70	ns
Chip Enable Access Time	t_{CE}	-	55	-	60	-	65	-	70	ns
Output Enable Time	t_{OE}	-	20	-	25	-	30	-	30	ns
Page Read Cycle Time (1)	t_{PRC}	20	-	25	-	25	-	30	-	ns
Page Address Access Time	t_{PA}	-	20	-	25	-	25	-	30	ns
$\overline{CE}$ & $\overline{OE}$ Disable Time (1)	t_{DF}	-	16	-	16	-	16	-	16	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$ (1)	t_{OH}	5	-	5	-	5	-	5	-	ns

Note : 1. Not 100% tested.

AC CHARACTERISTICS
Write(Erase/Program)Operations
Alternate $\overline{WE}$ Controlled Write

Parameter		Symbol	Vcc=2.7V ~ 3.6V								Unit
			4A		4B		4C		4D		
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time (1)		tWC	55	-	60	-	65	-	70	-	ns
Address Setup Time		tAS	0	-	0	-	0	-	0	-	ns
		tASO	15	-	15	-	15	-	15	-	ns
Address Hold Time		tAH	30	-	35	-	35	-	35	-	ns
		tAHT	0	-	0	-	0	-	0	-	ns
Data Setup Time		tDS	25	-	30	-	30	-	30	-	ns
Data Hold Time		tDH	0	-	0	-	0	-	0	-	ns
Output Enable Setup Time (1)		tOES	0	-	0	-	0	-	0	-	ns
Output Enable Hold	Read (1)	tOEH1	0	-	0	-	0	-	0	-	ns
	Toggle and $\overline{Data}$ Polling (1)	tOEH2	10	-	10	-	10	-	10	-	ns
$\overline{CE}$ Setup Time		tCS	0	-	0	-	0	-	0	-	ns
$\overline{CE}$ Hold Time		tCH	0	-	0	-	0	-	0	-	ns
Write Pulse Width		tWP	35	-	35	-	35	-	35	-	ns
Write Pulse Width High		tWPH	20	-	25	-	25	-	25	-	ns
Programming Operation		tPGM	6(typ.)		6(typ)		6(typ.)		6(typ.)		µs
Accelerated Programming Operation		tACCPGM	4(typ.)		4(typ)		4(typ.)		4(typ.)		µs
Accelerated Quad word Programming Operation		tACCPGM_QUAD	1.2(typ.)		1.2(typ.)		1.2(typ.)		1.2(typ.)		µs
Block Erase Operation (2)		tBERS	0.7(typ.)		0.7(typ)		0.7(typ.)		0.7(typ.)		sec
Vcc Set Up Time		tVCS	50	-	50	-	50	-	50	-	µs
Write Recovery Time from RY/$\overline{BY}$		tRB	0	-	0	-	0	-	0	-	ns
$\overline{RESET}$ High Time Before Read		tRH	50	-	50	-	50	-	50	-	ns
$\overline{RESET}$ to Power Down Time		tRPD	20	-	20	-	20	-	20	-	µs
Program/Erase Valid to RY/$\overline{BY}$ Delay		tBUSY	35	90	35	90	35	90	35	90	ns
VID Rising and Falling Time		tVID	500	-	500	-	500	-	500	-	ns
$\overline{RESET}$ Pulse Width		tRP	500	-	500	-	500	-	500	-	ns
$\overline{RESET}$ Low to RY/BY High		tRRB	-	20	-	20	-	20	-	20	µs
$\overline{RESET}$ Setup Time for Temporary Unprotect		tRSP	4	-	4	-	4	-	4	-	µs
$\overline{RESET}$ Low Setup Time		tRSTS	500	-	500	-	500	-	500	-	ns
$\overline{RESET}$ High to Address Valid		tRSTW	200	-	200	-	200	-	200	-	ns
Read Recovery Time Before Write		tGHWL	0	-	0	-	0	-	0	-	ns
$\overline{CE}$ High during toggling bit polling		tCEPH	20	-	20	-	20	-	20	-	ns
$\overline{OE}$ High during toggling bit polling		tOEPH	10	-	10	-	10	-	10	-	ns

Notes : 1. Not 100% tested.
2. The duration of the Program or Erase operation varies and is calculated in the internal algorithms.

AC CHARACTERISTICS
Write(Erase/Program)Operations
Alternate $\overline{CE}$ Controlled Writes

Parameter		Symbol	Vcc=2.7V ~ 3.6V								Unit
			4A		4B		4C		4D		
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time (1)		tWC	55	-	60	-	65	-	70	-	ns
Address Setup Time		tAS	0	-	0	-	0	-	0	-	ns
Address Hold Time		tAH	30	-	35	-	35	-	35	-	ns
Data Setup Time		tDS	25	-	30	-	30	-	30	-	ns
Data Hold Time		tDH	0	-	0	-	0	-	0	-	ns
Output Enable Setup Time (1)		tOES	0	-	0	-	0	-	0	-	ns
Output Enable Hold Time	Read (1)	tOEH1	0	-	0	-	0	-	0	-	ns
	Toggle and $\overline{Data}$ Polling (1)	tOEH2	10	-	10	-	10	-	10	-	ns
$\overline{WE}$ Setup Time		tWS	0	-	0	-	0	-	0	-	ns
$\overline{WE}$ Hold Time		tWH	0	-	0	-	0	-	0	-	ns
$\overline{CE}$ Pulse Width		tCP	35	-	40	-	40	-	40	-	ns
$\overline{CE}$ Pulse Width High		tCPH	20	-	25	-	25	-	25	-	ns
Programming Operation		tPGM	6(typ.)		6(typ)		6(typ.)		6(typ.)		µs
Accelerated Programming Operation		tACCPGM	4(typ.)		4(typ)		4typ.)		4(typ.)		µs
Accelerated Quad word Programming Operation		tACCPGM_QUAD	1.2(typ.)		1.2(typ.)		1.2(typ.)		1.2(typ.)		µs
Block Erase Operation (2)		tBERS	0.7(typ.)		0.7(typ)		0.7typ.)		0.7(typ.)		sec

Notes : 1. Not 100% tested.
2.This does not include the preprogramming time.

ERASE AND PROGRAM PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max		
Block Erase Time	-	0.7	2	sec	Excludes 00H programming prior to erasure
Chip Erase Time	-	135	216	sec	
Word Programming Time	-	6	100	µs	Excludes system-level overhead
Accelerated Word Program Time	-	4	60	µs	Excludes system-level overhead
Accelerated Quad Word Program Time	-	1.2	-	µs	Excludes system-level overhead
Chip Programming Time	-	50.4	200	sec	Excludes system-level overhead
Erase/Program Endurance	100,000	-	-	cycles	Minimum 100,000 cycles guaranteed

Notes : 1. 25 °C, Vcc = 3.0V 100,000 cycles, typical pattern.
2. System-level overhead is defined as the time required to execute the four bus cycle command necessary to program each word.
In the preprogramming step of the Internal Erase Routine, all words are programmed to 00H before erasure.

SWITCHING WAVEFORMS

Conventional Read Operations

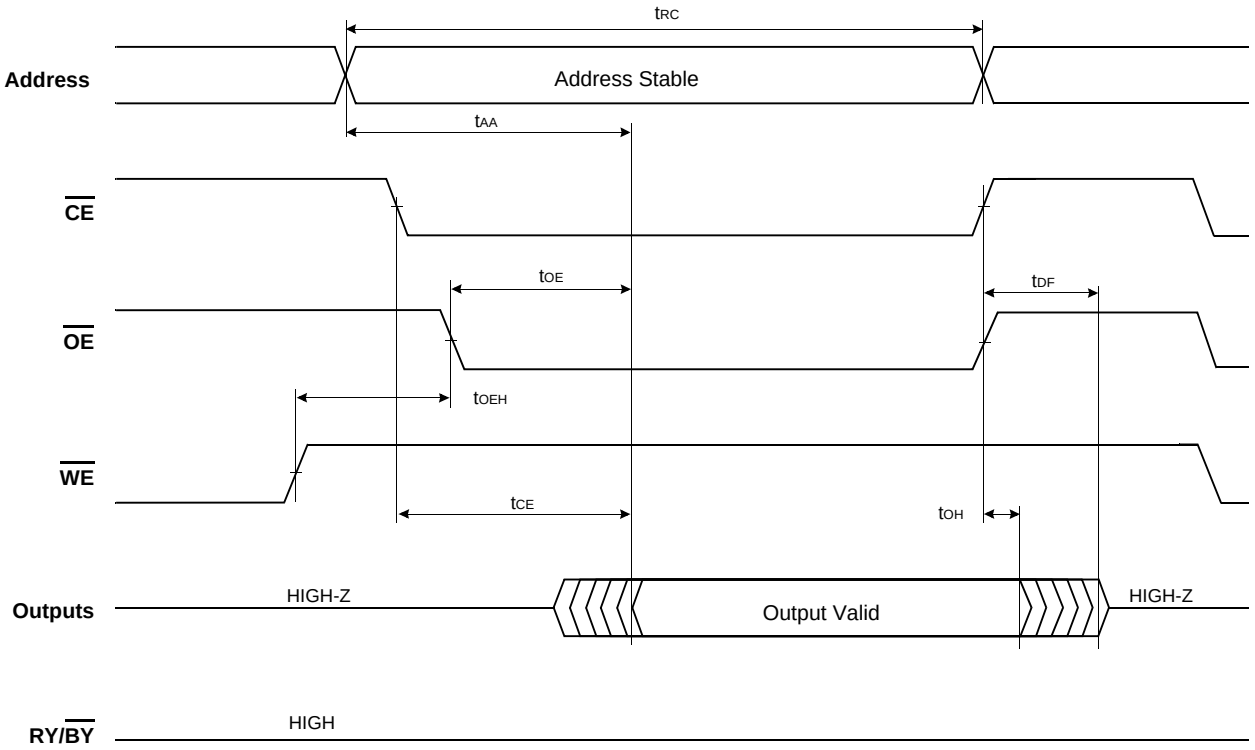


Figure 10. Conventional Read Operation Timings

Parameter	Symbol	4A		4B		4C		4D		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	55	-	60	-	65	-	70	-	ns
Address Access Time	tAA	-	55	-	60	-	65	-	70	ns
Chip Enable Access Time	tCE	-	55	-	60	-	65	-	70	ns
Output Enable Time	tOE	-	20	-	25	-	30	-	30	ns
$\overline{CE}$ & $\overline{OE}$ Disable Time (1)	tDF	-	16	-	16	-	16	-	16	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$	tOH	5	-	5	-	5	-	5	-	ns
$\overline{OE}$ Hold Time	tOEH	0	10	0	10	0	10	0	10	ns

Note : 1. Not 100% tested.

SWITCHING WAVEFORMS

Page Read Operations

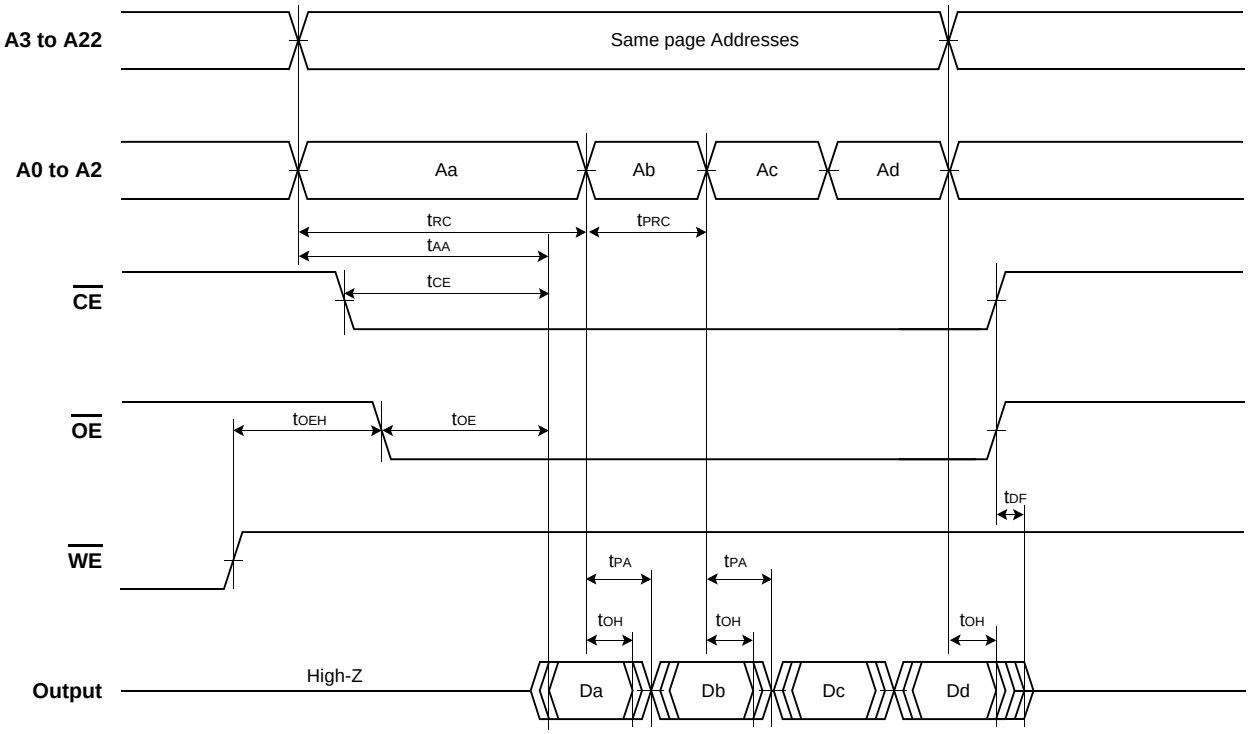


Figure 11. Page Read Operation Timings

Parameter	Symbol	4A		4B		4C		4D		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	55	-	60	-	65	-	70	-	ns
Page Read Cycle Time	t_{PRC}	20	-	25	-	25	-	30	-	ns
Address Access Time	t_{AA}	-	55	-	60	-	65	-	70	ns
Page Address Access Time	t_{PA}	-	20	-	25	-	25	-	30	ns
Chip Enable Access Time	t_{CE}	-	55	-	60	-	65	-	70	ns
Output Enable Time	t_{OE}	-	20	-	25	-	30	-	30	ns
$\overline{CE}$ & $\overline{OE}$ Disable Time (1)	t_{DF}	-	16	-	16	-	16	-	16	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$	t_{OH}	5	-	5	-	5	-	5	-	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	-	0	-	0	-	0	-	ns

Note : 1. Not 100% tested.

SWITCHING WAVEFORMS
Hardware Reset/Read Operations

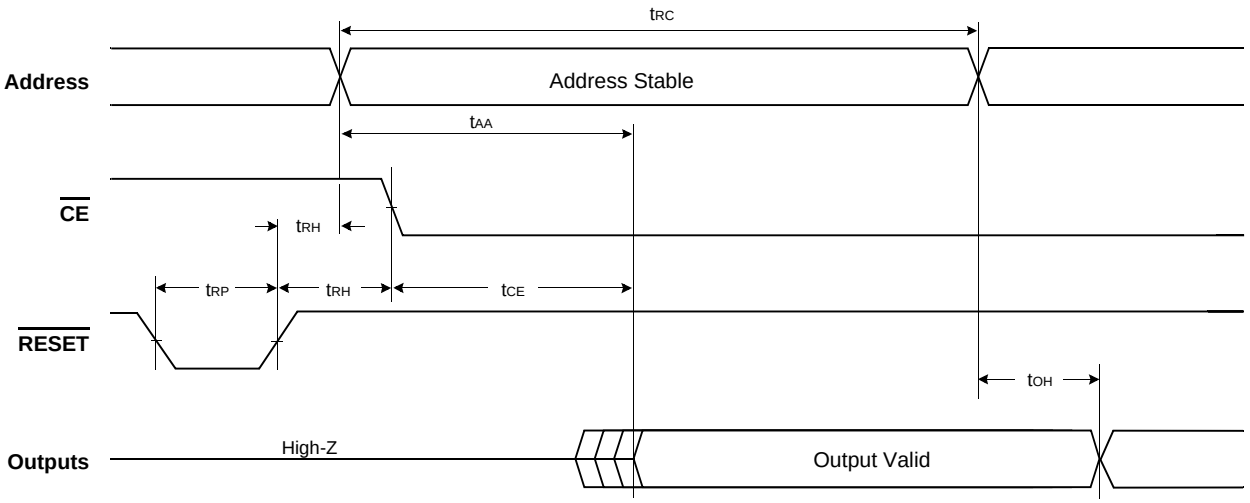
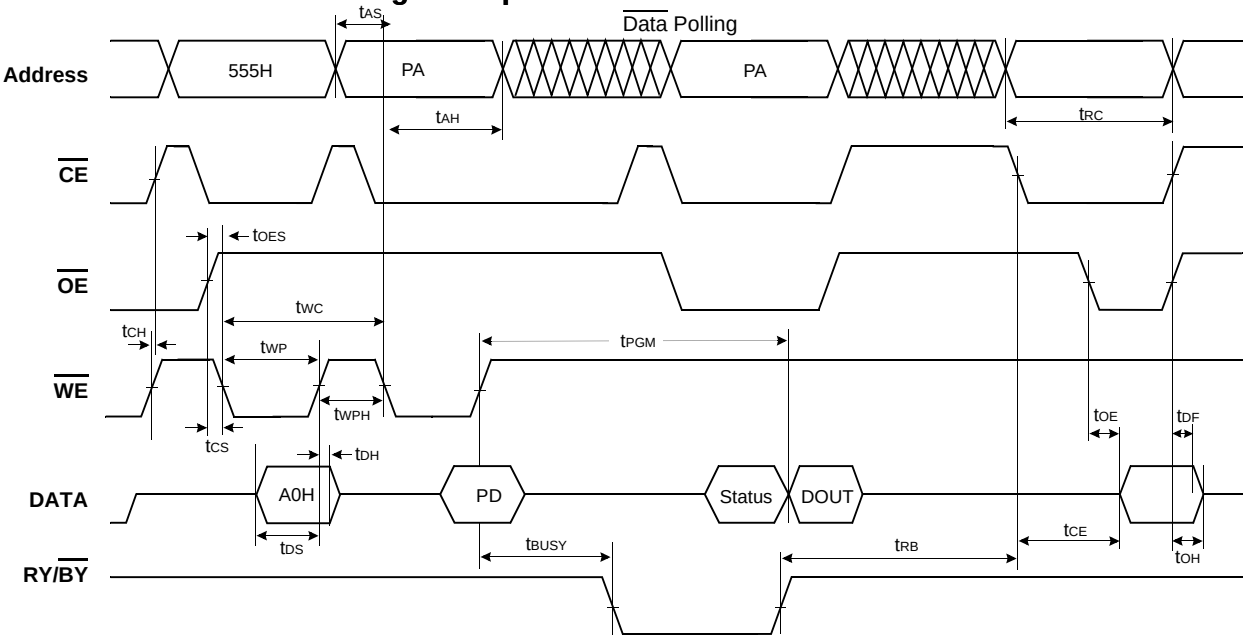


Figure 12. Hardware Reset/Read Operation Timings

Parameter	Symbol	4A		4B		4C		4D		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	55	-	60	-	65	-	70	-	ns
Address Access Time	t_{AA}	-	55	-	60	-	65	-	70	ns
Chip Enable Access Time	t_{CE}	-	55	-	60	-	65	-	70	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$	t_{OH}	5	-	5	-	5	-	5	-	ns
$\overline{RESET}$ Pulse Width	t_{RP}	500	-	500	-	500	-	500	-	ns
$\overline{RESET}$ High Time Before Read	t_{RH}	50	-	50	-	50	-	50	-	ns

SWITCHING WAVEFORMS

Alternate $\overline{WE}$ Controlled Program Operations



Notes : 1. $\overline{DQ7}$ is the output of the complement of the data written to the device.
2. DOUT is the output of the data written to the device.
3. PA : Program Address, PD : Program Data
4. The illustration shows the last two cycles of the program command sequence.

Figure 13. Alternate $\overline{WE}$ Controlled Program Operation Timings

Parameter	Symbol	4A		4B		4C		4D		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	55	-	60	-	65	-	70	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	0	-	ns
Address Hold Time	tAH	30	-	35	-	35	-	35	-	ns
Data Setup Time	tDS	25	-	30	-	30	-	30	-	ns
Data Hold Time	tDH	0	-	0	-	0	-	0	-	ns
$\overline{CE}$ Setup Time	tCS	0	-	0	-	0	-	0	-	ns
$\overline{CE}$ Hold Time	tCH	0	-	0	-	0	-	0	-	ns
$\overline{OE}$ Setup Time	tOES	0	-	0	-	0	-	0	-	ns
Write Pulse Width	tWP	35	-	35	-	35	-	35	-	ns
Write Pulse Width High	tWPH	20	-	25	-	25	-	25	-	ns
Programming Operation	tPGM	6(typ.)		6(typ)		6(typ.)		6(typ.)		us
Accelerated Programming Operation	tACCPGM	4(typ.)		4(typ)		4(typ.)		4(typ.)		μs
Read Cycle Time	tRC	55	-	60	-	65	-	70	-	ns
Chip Enable Access Time	tCE	-	55	-	60	-	65	-	70	ns
Output Enable Time	tOE	-	20	-	25	-	30	-	30	ns
$\overline{CE}$ & $\overline{OE}$ Disable Time	tDF	-	16	-	16	-	16	-	16	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$	tOH	5	-	5	-	5	-	5	-	ns
Program/Erase Valid to RY/$\overline{BY}$ Delay	tBUSY	35	90	35	90	35	90	35	90	ns
Recovery Time from RY/$\overline{BY}$	tRB	0	-	0	-	0	-	0	-	ns

SWITCHING WAVEFORMS

Alternate $\overline{CE}$ Controlled Program Operations

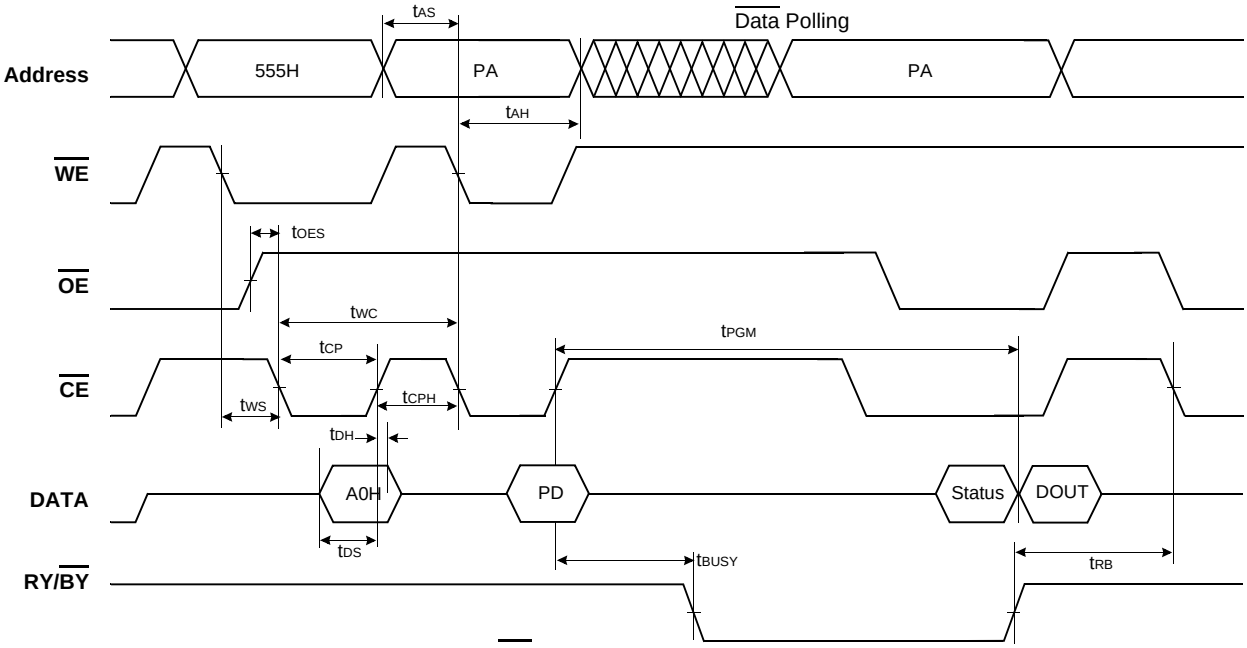


Figure 14. Alternate $\overline{CE}$ Controlled Program Operation Timings

Notes :
1. DQ7 is the output of the complement of the data written to the device.
2. DOUT is the output of the data written to the device.
3. PA : Program Address, PD : Program Data
4. The illustration shows the last two cycles of the program command sequence.

Parameter	Symbol	4A		4B		4C		4D		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	55	-	60	-	65	-	70	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	0	-	ns
Address Hold Time	tAH	30	-	35	-	35	-	35	-	ns
Data Setup Time	tDS	25	-	30	-	30	-	30	-	ns
Data Hold Time	tDH	0	-	0	-	0	-	0	-	ns
$\overline{OE}$ Setup Time	tOES	0	-	0	-	0	-	0	-	ns
$\overline{WE}$ Setup Time	tWS	0	-	0	-	0	-	0	-	ns
$\overline{WE}$ Hold Time	tWH	0	-	0	-	0	-	0	-	ns
$\overline{CE}$ Pulse Width	tCP	35	-	40	-	40	-	40	-	ns
$\overline{CE}$ Pulse Width High	tCPH	20	-	25	-	25	-	25	-	ns
Programming Operation	tPGM	6(typ.)		6(typ)		6(typ.)		6(typ.)		µs
Accelerated Programming Operation	tACCPGM	4(typ.)		4(typ)		4(typ.)		4(typ.)		µs
Program/Erase Valid to RY/$\overline{BY}$ Delay	tBUSY	35	90	35	90	35	90	35	90	ns
Recovery Time from RY/$\overline{BY}$	tRB	0	-	0	-	0	-	0	-	ns

SWITCHING WAVEFORMS

Chip/Block Erase Operations

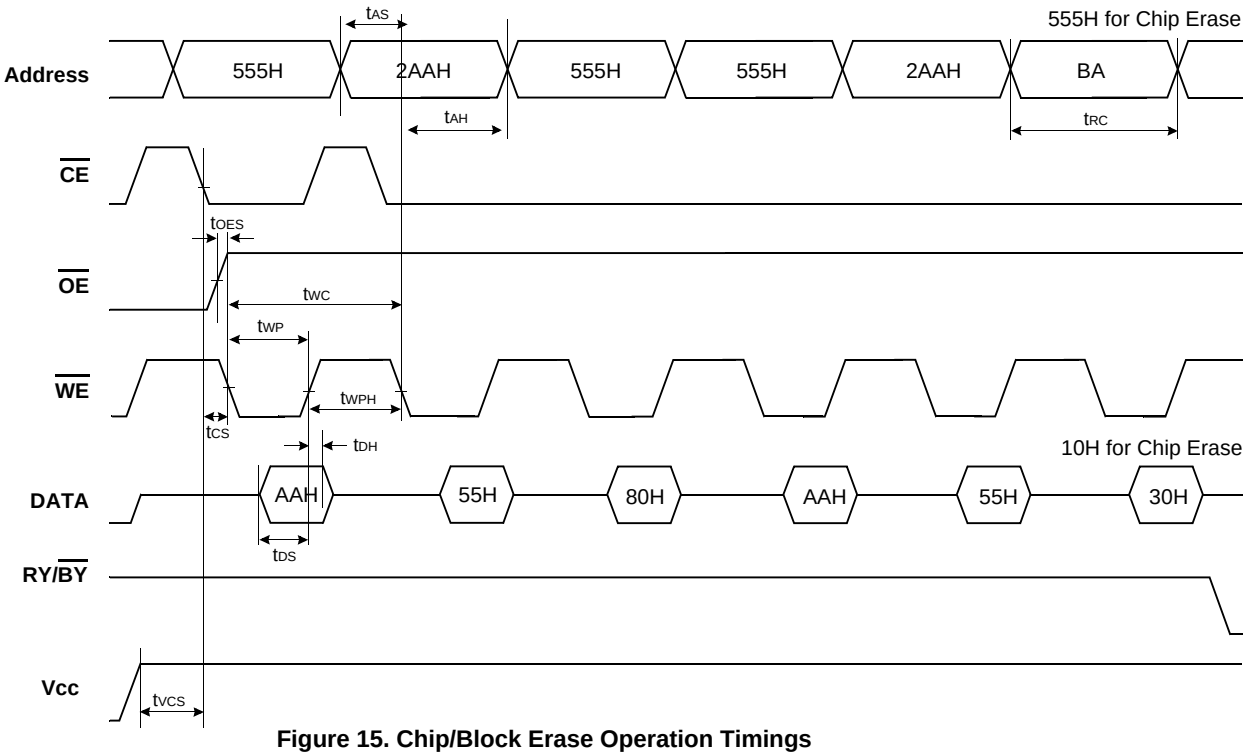


Figure 15. Chip/Block Erase Operation Timings

Note : BA : Block Address

Parameter	Symbol	4A		4B		4C		4D		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	55	-	60	-	65	-	70	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Address Hold Time	t_{AH}	30	-	35	-	35	-	35	-	ns
Data Setup Time	t_{DS}	25	-	30	-	30	-	30	-	ns
Data Hold Time	t_{DH}	0	-	0	-	0	-	0	-	ns
$\overline{OE}$ Setup Time	t_{OES}	0	-	0	-	0	-	0	-	ns
$\overline{CE}$ Setup Time	t_{CS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	35	-	35	-	35	-	35	-	ns
Write Pulse Width High	t_{WPH}	20	-	25	-	25	-	25	-	ns
Read Cycle Time	t_{RC}	55	-	60	-	65	-	70	-	ns
V_{CC} Set Up Time	t_{VCS}	50	-	50	-	50	-	50	-	μs

SWITCHING WAVEFORMS
Read While Write Operations

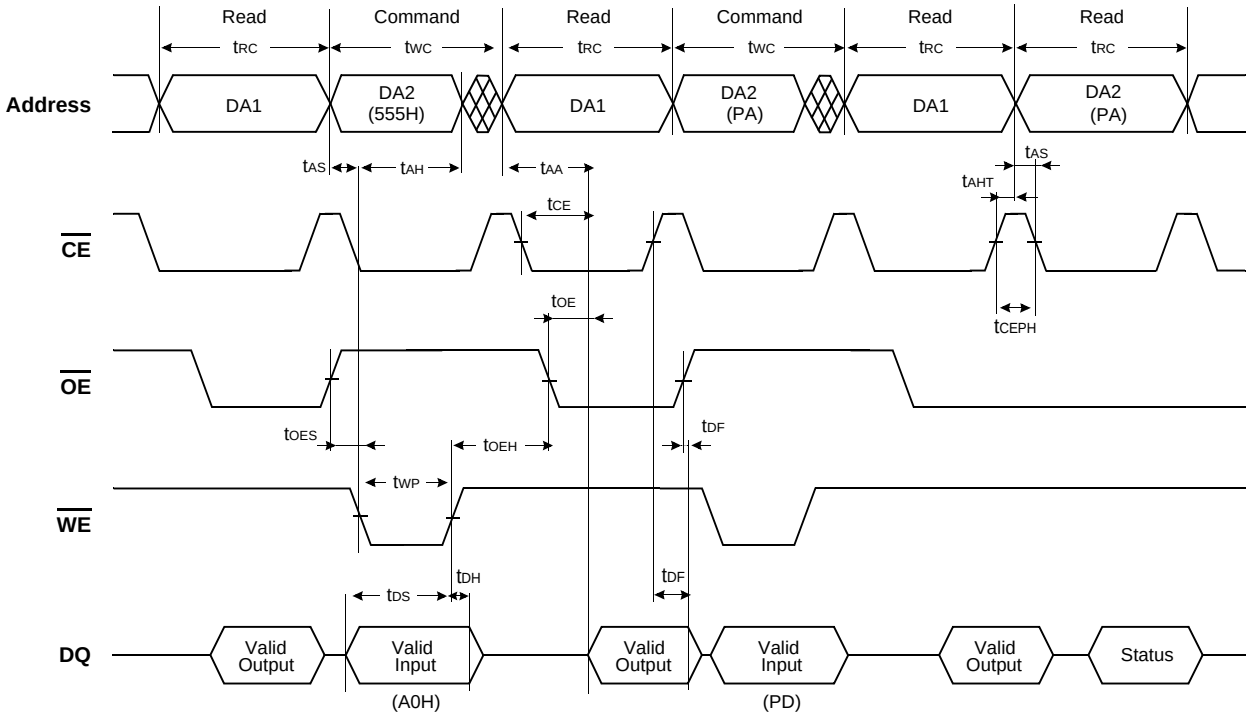


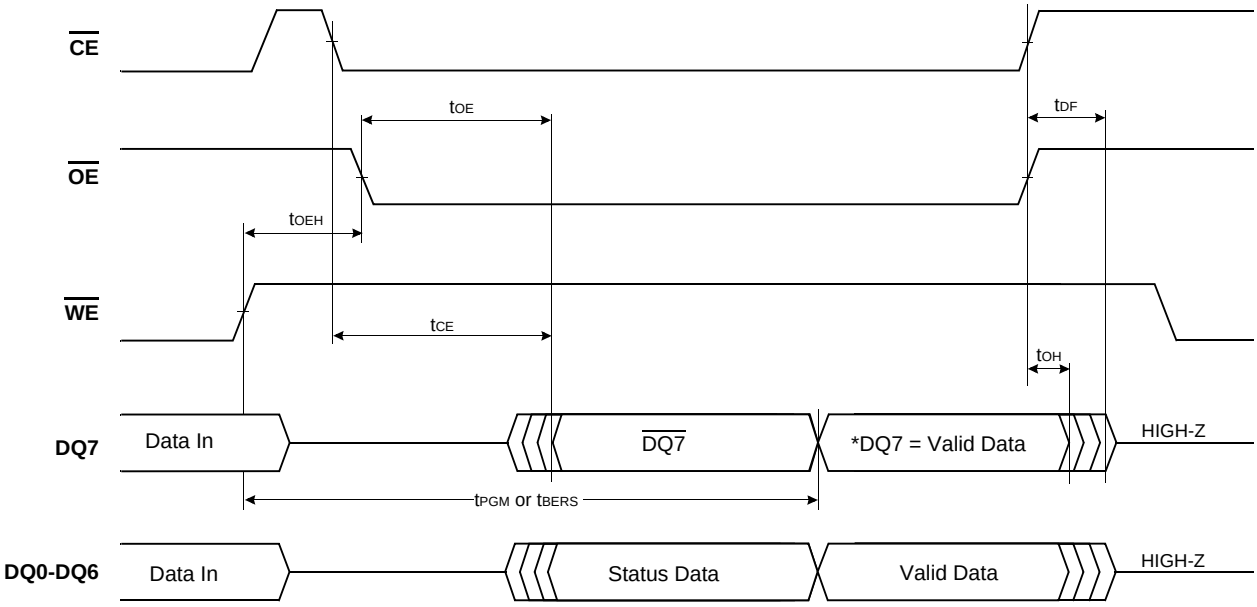
Figure 16. Read While Write Operation Timings

Note : This is an example in the program-case of the Read While Write function.
DA1 : Address of Bank1, DA2 : Address of Bank 2
PA = Program Address at one bank , RA = Read Address at the other bank, PD = Program Data In , RD = Read Data Out

Parameter	Symbol	4A		4B		4C		4D		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	55	-	60	-	65	-	70	-	ns
Write Pulse Width	t_{WP}	35	-	35	-	35	-	35	-	ns
Write Pulse Width High	t_{WPH}	20	-	25	-	25	-	25	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Address Hold Time	t_{AH}	30	-	35	-	35	-	35	-	ns
Data Setup Time	t_{DS}	25	-	30	-	30	-	30	-	ns
Data Hold Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Read Cycle Time	t_{RC}	55	-	60	-	65	-	70	-	ns
Chip Enable Access Time	t_{CE}	-	55	-	60	-	65	-	70	ns
Address Access Time	t_{AA}	-	55	-	60	-	65	-	70	ns
Output Enable Access Time	t_{OE}	-	20	-	25	-	30	-	30	ns
$\overline{OE}$ Setup Time	t_{OES}	0	-			0	-	0	-	ns
$\overline{OE}$ Hold Time	t_{OEH}	10	-	10	-	10	-	10	-	ns
$\overline{CE}$ & $\overline{OE}$ Disable Time	t_{DF}	-	16	-	16	-	16	-	16	ns
Address Hold Time	t_{AHT}	30	-	35	-	35	-	35	-	ns
$\overline{CE}$ High during toggle bit polling	t_{CEPH}	20	-	20	-	20	-	20	-	ns

SWITCHING WAVEFORMS

Data Polling During Internal Routine Operation



Note : *DQ7=Vaild Data (The device has completed the internal operation).

Figure 17. Data Polling During Internal Routine Operation Timings

RY/BY Timing Diagram During Program/Erase Operation

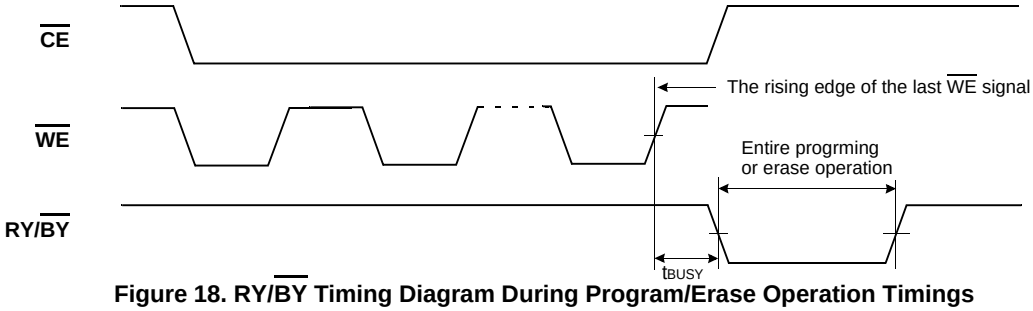
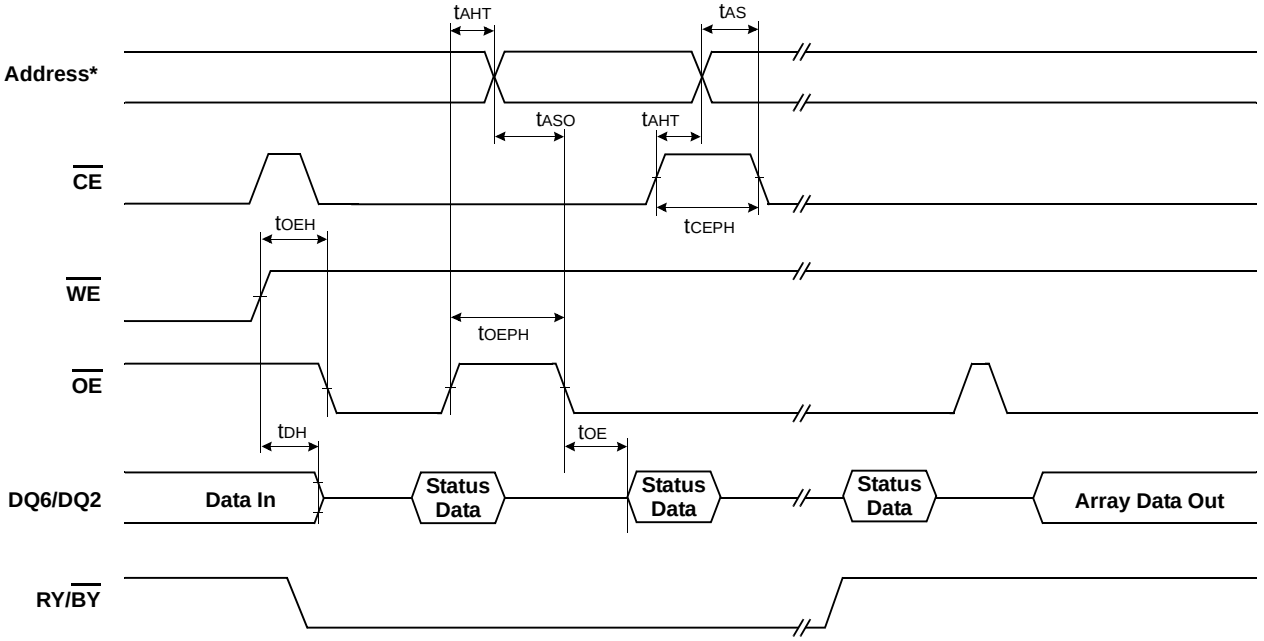


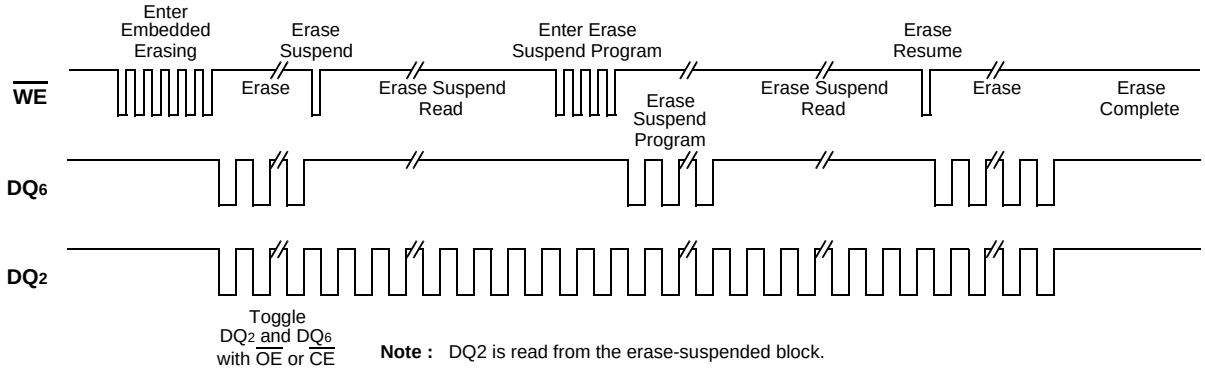
Figure 18. RY/BY Timing Diagram During Program/Erase Operation Timings

Parameter	Symbol	4A		4B		4C		4D		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Program/Erase Valid to RY/BY Delay	tBUSY	35	90	35	90	35	90	35	90	ns
Chip Enable Access Time	tCE	-	55	-	60	-	65	-	70	ns
Output Enable Time	tOE	-	20	-	25	-	30	-	30	ns
CE & OE Disable Time	tDF	-	16	-	16	-	16	-	16	ns
Output Hold Time from Address, CE or OE	tOH	5	-	5	-	5	-	5	-	ns
OE Hold Time	tOEH	10	-	10	-	10	-	10	-	ns

SWITCHING WAVEFORMS
Toggle Bit During Internal Routine Operation



Note : Address for the write operation must include a bank address (A19~A22) where the data is written.



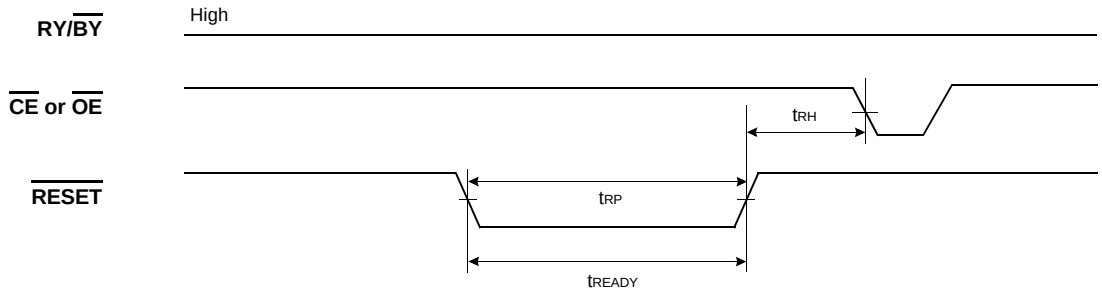
Note : DQ2 is read from the erase-suspended block.

Figure 19. Toggle Bit During Internal Routine Operation Timings

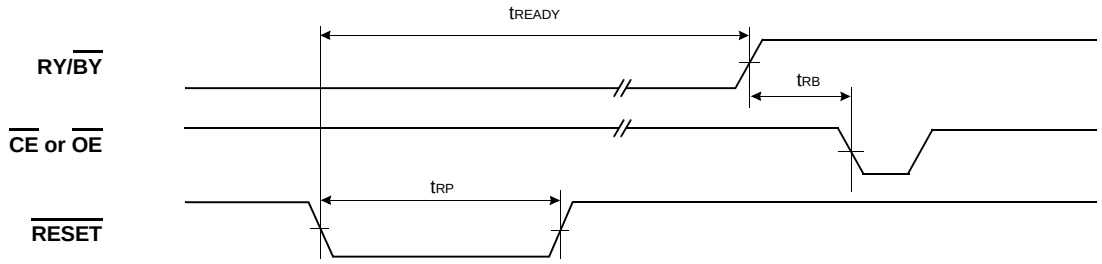
Parameter	Symbol	4A		4B		4C		4D		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Enable Access Time	tOE	-	20	-	25	-	30	-	30	ns
$\overline{OE}$ Hold Time	tOEH	10	-	10	-	10	-	10	-	ns
Address Hold Time	tAHT	30	-	35	-	35	-	35	-	ns
Address Setup	tASO	55	-	55	-	55	-	55	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	0	-	ns
Data Hold Time	tDH	0	-	0	-	0	-	0	-	ns
$\overline{CE}$ High during toggle bit polling	tCEPH	20	-	20	-	20	-	20	-	ns
$\overline{OE}$ High during toggle bit polling	tOEPH	10	-	10	-	10	-	10	-	ns

SWITCHING WAVEFORMS

RESET Timing Diagram



Reset Timings NOT during Internal Routine



Reset Timings during Internal Routine

Power-up and RESET Timing Diagram

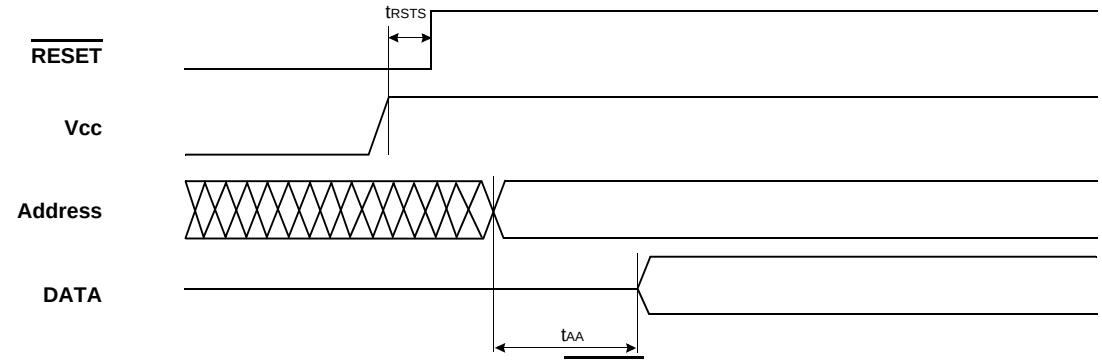
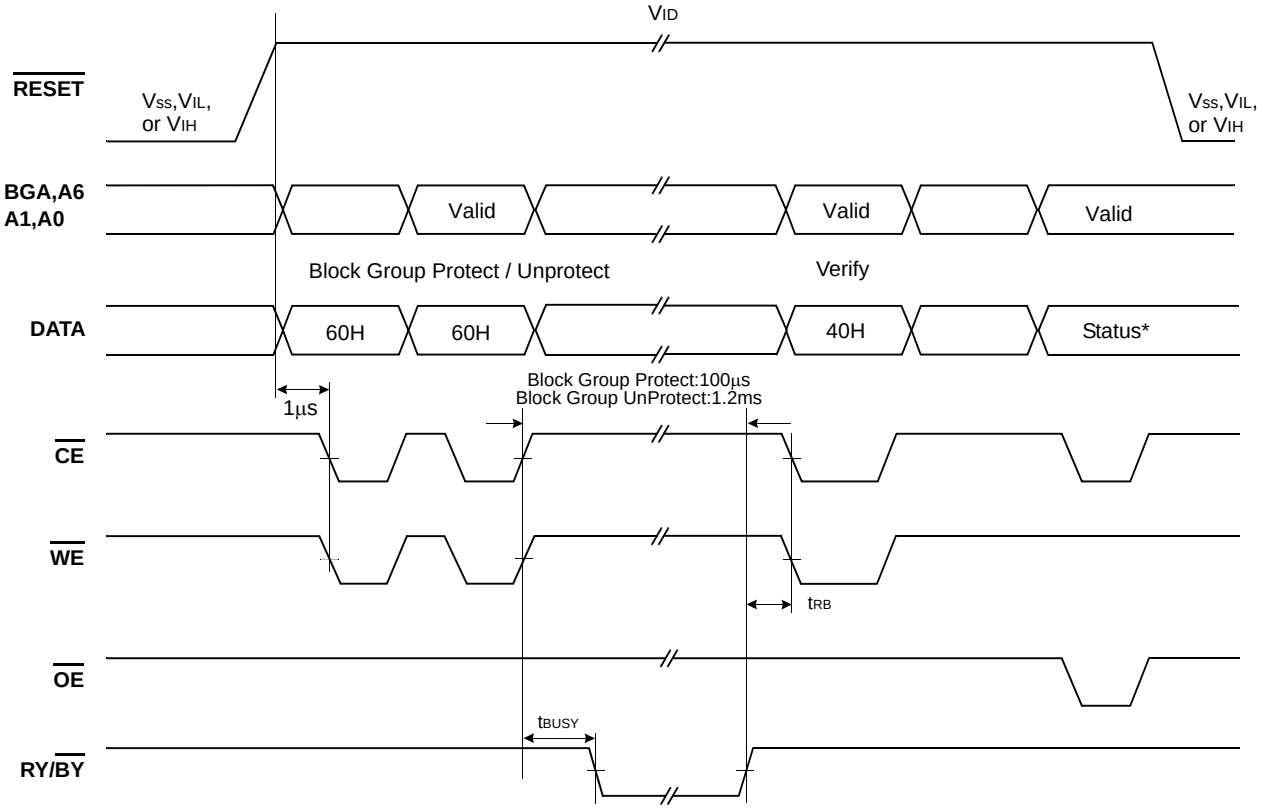


Figure 20. Power-up and RESET Timing Diagram

Parameter	Symbol	4A		4B		4C		4D		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
RESET Pulse Width	tRP	500	-	500	-	500	-	500	-	ns
RESET Low to Valid Data (During Internal Routine)	tREADY	-	20	-	20	-	20	-	20	µs
RESET Low to Valid Data (Not during Internal Routine)	tREADY	-	500	-	500	-	500	-	500	ns
RESET High Time Before Read	tRH	50	-	50	-	50	-	50	-	ns
RY/BY Recovery Time	tRB	0	-	0	-	0	-	0	-	ns
RESET High to Address Valid	tRSTW	200	-	200	-	200	-	200	-	ns
RESET Low Set-up Time	tRSTS	500	-	500	-	500	-	500	-	ns

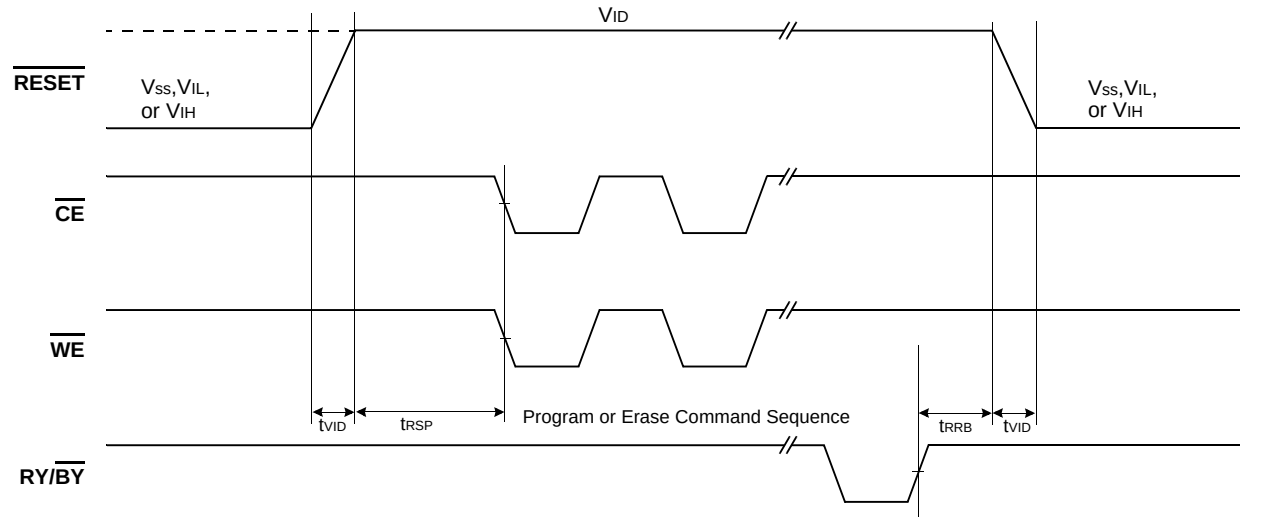
SWITCHING WAVEFORMS

Block Group Protect & Unprotect Operations



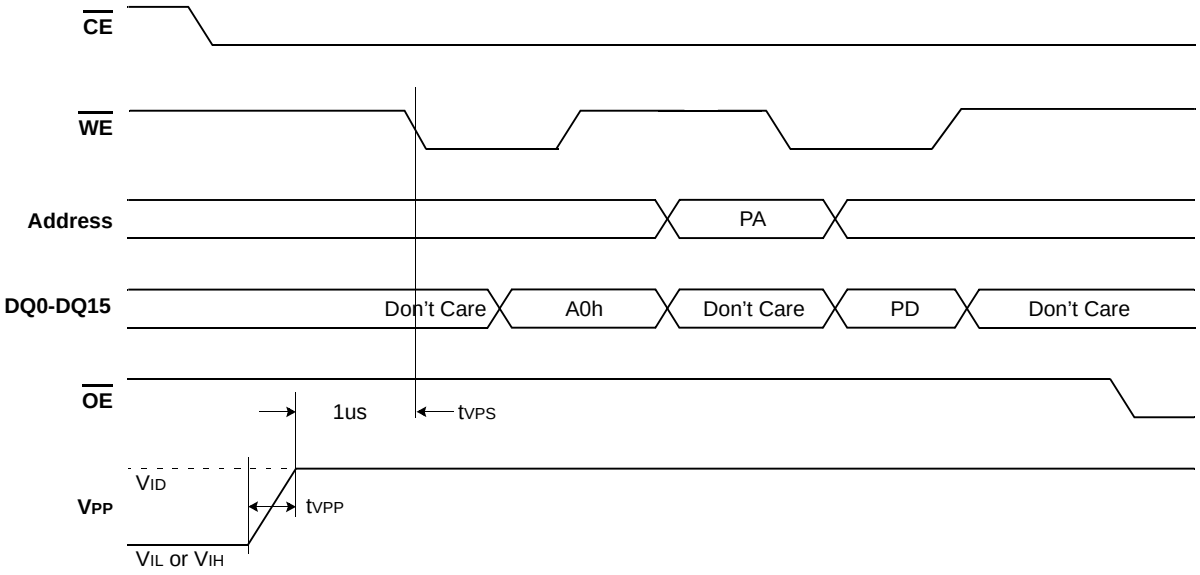
Notes : Block Group Protect (A6=V_{IL} , A1=V_{IH} , A0=V_{IL}) , Status=01H
Block Group Unprotect (A6=V_{IH} , A1=V_{IH}, A0=V_{IL}) , Status=00H
BGA = Block Group Address (A12 ~ A22)

Temporary Block Group Unprotect

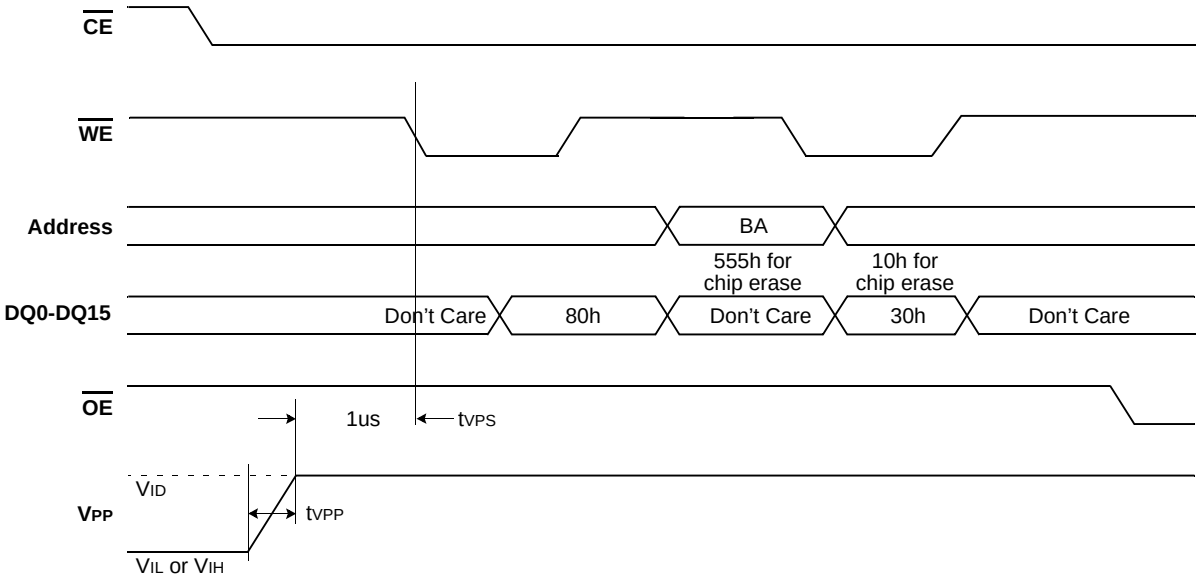


SWITCHING WAVEFORMS

Unlock Bypass Program Operations(Accelerated Program)



Unlock Bypass Block Erase Operations



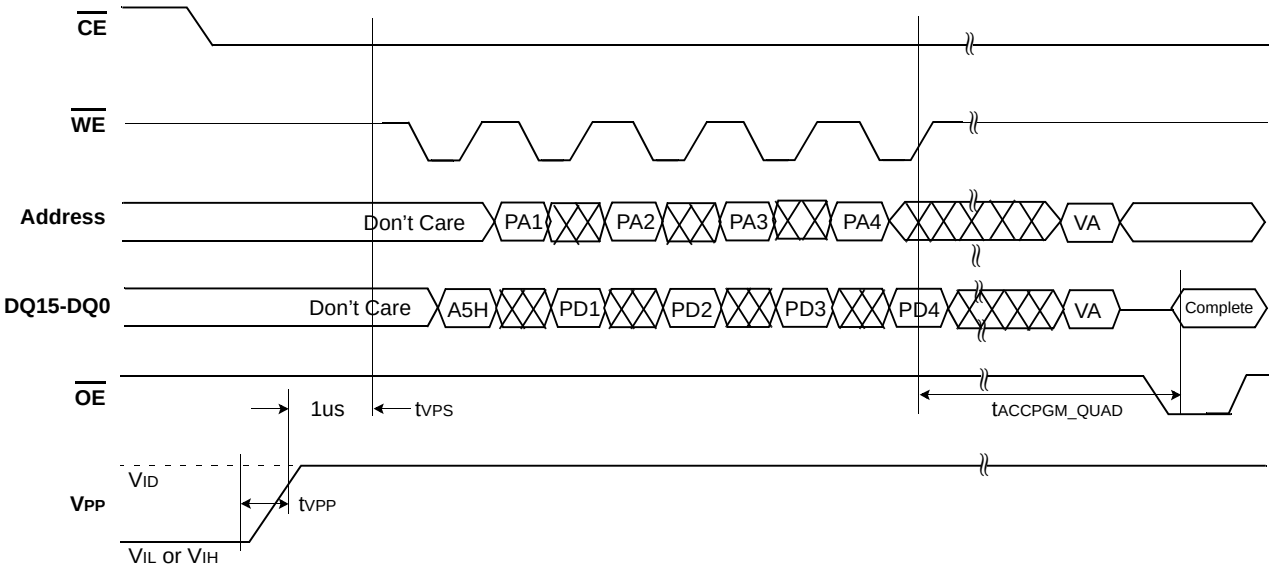
Notes:

1. V_{PP} can be left high for subsequent programming pulses.
2. Use setup and hold times from conventional program operations.
3. Unlock Bypass Program/Erase commands can be used when the V_{ID} is applied to Vpp.

Figure 21. Unlock Bypass Operation Timings

SWITCHING WAVEFORMS

Quad word Accelerated Program



Notes:

1. V_{PP} can be left high for subsequent programming pulses.
2. Use setup and hold times from conventional program operations.
3. Quad word Acelerate program commands can be used when the V_{ID} is applied to Vpp.

Figure 22. Quad word Accelerated Program Operation Timings

Table 13. Block Architecture

Bank	Block	Block Size	(x16) Address Range
Bank 3	BA269	4 Kwords	7FF000h-7FFFFFh
	BA268	4 Kwords	7FE000h-7FEFFFh
	BA267	4 Kwords	7FD000h-7FDFFFh
	BA266	4 Kwords	7FC000h-7FCFFFh
	BA265	4 Kwords	7FB000h-7FBFFFh
	BA264	4 Kwords	7FA000h-7FAFFFh
	BA263	4 Kwords	7F9000h-7F9FFFh
	BA262	4 Kwords	7F8000h-7F8FFFh
	BA261	32 Kwords	7F0000h-7F7FFFh
	BA260	32 Kwords	7E8000h-7EFFFFh
	BA259	32 Kwords	7E0000h-7E7FFFh
	BA258	32 Kwords	7D8000h-7DFFFFh
	BA257	32 Kwords	7D0000h-7D7FFFh
	BA256	32 Kwords	7C8000h-7CFFFFh
	BA255	32 Kwords	7C0000h-7C7FFFh
	BA254	32 Kwords	7B8000h-7BFFFFh
	BA253	32 Kwords	7B0000h-7B7FFFh
	BA252	32 Kwords	7A8000h-7AFFFFh
	BA251	32 Kwords	7A0000h-7A7FFFh
	BA250	32 Kwords	798000h-79FFFFh
	BA249	32 Kwords	790000h-797FFFh
	BA248	32 Kwords	788000h-78FFFFh
	BA247	32 Kwords	780000h-787FFFh
	BA246	32 Kwords	778000h-77FFFFh
	BA245	32 Kwords	770000h-777FFFh
	BA244	32 Kwords	768000h-76FFFFh
	BA243	32 Kwords	760000h-767FFFh
	BA242	32 Kwords	758000h-75FFFFh
	BA241	32 Kwords	750000h-757FFFh
	BA240	32 Kwords	748000h-74FFFFh
	BA239	32 Kwords	740000h-747FFFh
	BA238	32 Kwords	738000h-73FFFFh
	BA237	32 Kwords	730000h-737FFFh
	BA236	32 Kwords	728000h-72FFFFh
	BA235	32 Kwords	720000h-727FFFh
	BA234	32 Kwords	718000h-71FFFFh
	BA233	32 Kwords	710000h-717FFFh
	BA232	32 Kwords	708000h-70FFFFh
	BA231	32 kwords	700000h-707FFFh
	BA230	32 Kwords	6F8000h-6FFFFFh
	BA229	32 Kwords	6F0000h-6F7FFFh
	BA228	32 Kwords	6E8000h-6EFFFFh
	BA227	32 Kwords	6E0000h-6E7FFFh
	BA226	32 Kwords	6D8000h-6DFFFFh

Table 13. Block Architecture

Bank	Block	Block Size	(x16) Address Range
Bank 2	BA225	32 Kwords	6D0000h-6D7FFFh
	BA224	32 Kwords	6C8000h-6CFFFFh
	BA223	32 Kwords	6C0000h-6C7FFFh
	BA222	32 Kwords	6B8000h-6BFFFFh
	BA221	32 Kwords	6B0000h-6B7FFFh
	BA220	32 Kwords	6A8000h-6AFFFFh
	BA219	32 Kwords	6A0000h-6A7FFFh
	BA218	32 Kwords	698000h-69FFFFh
	BA217	32 Kwords	690000h-697FFFh
	BA216	32 Kwords	688000h-68FFFFh
	BA215	32 Kwords	680000h-687FFFh
	BA214	32 Kwords	678000h-67FFFFh
	BA213	32 Kwords	670000h-677FFFh
	BA212	32 Kwords	668000h-66FFFFh
	BA211	32 Kwords	660000h-667FFFh
	BA210	32 Kwords	658000h-65FFFFh
	BA209	32 Kwords	650000h-657FFFh
	BA208	32 Kwords	648000h-64FFFFh
	BA207	32 Kwords	640000h-647FFFh
	BA206	32 Kwords	638000h-63FFFFh
	BA205	32 Kwords	630000h-637FFFh
	BA204	32 Kwords	628000h-62FFFFh
	BA203	32 Kwords	620000h-627FFFh
	BA202	32 Kwords	618000h-61FFFFh
	BA201	32 Kwords	610000h-617FFFh
	BA200	32 Kwords	608000h-60FFFFh
	BA199	32 Kwords	600000h-607FFFh
	BA198	32 Kwords	5F8000h-5FFFFFh
	BA197	32 Kwords	5F0000h-5F7FFFh
	BA196	32 Kwords	5E8000h-5EFFFFh
	BA195	32 Kwords	5E0000h-5E7FFFh
	BA194	32 Kwords	5D8000h-5DFFFFh
	BA193	32 Kwords	5D0000h-5D7FFFh
	BA192	32 Kwords	5C8000h-5CFFFFh
	BA191	32 Kwords	5C0000h-5C7FFFh
	BA190	32 Kwords	5B8000h-5BFFFFh
	BA189	32 Kwords	5B0000h-5B7FFFh
	BA188	32 Kwords	5A8000h-5AFFFFh
	BA187	32 Kwords	5A0000h-5A7FFFh
	BA186	32 Kwords	598000h-59FFFFh
	BA185	32 Kwords	590000h-597FFFh
	BA184	32 Kwords	588000h-58FFFFh
	BA183	32 Kwords	580000h-587FFFh
	BA182	32 Kwords	578000h-57FFFFh

Table 13. Block Architecture

Bank	Block	Block Size	(x16) Address Range
Bank 2	BA181	32 Kwords	570000h-577FFFh
	BA180	32 Kwords	568000h-56FFFFh
	BA179	32 Kwords	560000h-567FFFh
	BA178	32 Kwords	558000h-55FFFFh
	BA177	32 Kwords	550000h-557FFFh
	BA176	32 Kwords	548000h-54FFFFh
	BA175	32 Kwords	540000h-547FFFh
	BA174	32 Kwords	538000h-53FFFFh
	BA173	32 Kwords	530000h-537FFFh
	BA172	32 Kwords	528000h-52FFFFh
	BA171	32 Kwords	520000h-527FFFh
	BA170	32 Kwords	518000h-51FFFFh
	BA169	32 Kwords	510000h-517FFFh
	BA168	32 Kwords	508000h-50FFFFh
	BA167	32 Kwords	500000h-507FFFh
	BA166	32 Kwords	4F8000h-4FFFFFh
	BA165	32 Kwords	4F0000h-4F7FFFh
	BA164	32 Kwords	4E8000h-4EFFFFh
	BA163	32 Kwords	4E0000h-4E7FFFh
	BA162	32 Kwords	4D8000h-4DFFFFh
	BA161	32 Kwords	4D0000h-4D7FFFh
	BA160	32 Kwords	4C8000h-4CFFFFh
	BA159	32 Kwords	4C0000h-4C7FFFh
	BA158	32 Kwords	4B8000h-4BFFFFh
	BA157	32 Kwords	4B0000h-4B7FFFh
	BA156	32 Kwords	4A8000h-4AFFFFh
	BA155	32 Kwords	4A0000h-4A7FFFh
	BA154	32 Kwords	498000h-49FFFFh
	BA153	32 Kwords	490000h-497FFFh
	BA152	32 Kwords	488000h-48FFFFh
	BA151	32 Kwords	480000h-487FFFh
	BA150	32 Kwords	478000h-47FFFFh
	BA149	32 Kwords	470000h-477FFFh
	BA148	32 Kwords	468000h-46FFFFh
	BA147	32 Kwords	460000h-467FFFh
	BA146	32 Kwords	458000h-45FFFFh
	BA145	32 Kwords	450000h-457FFFh
	BA144	32 Kwords	448000h-44FFFFh
	BA143	32 Kwords	440000h-447FFFh
	BA142	32 Kwords	438000h-43FFFFh
	BA141	32 Kwords	430000h-437FFFh
	BA140	32 Kwords	428000h-42FFFFh
	BA139	32 Kwords	420000h-427FFFh
	BA138	32 Kwords	418000h-41FFFFh
	BA137	32 Kwords	410000h-417FFFh

Table 13. Block Architecture

Bank	Block	Block Size	(x16) Address Range
Bank 2	BA136	32 Kwords	408000h-40FFFFh
	BA135	32 Kwords	400000h-407FFFh
Bank 1	BA134	32 Kwords	3F8000h-3FFFFFh
	BA133	32 Kwords	3F0000h-3F7FFFh
	BA132	32 Kwords	3E8000h-3EFFFFh
	BA131	32 Kwords	3E0000h-3E7FFFh
	BA130	32 Kwords	3D8000h-3DFFFFh
	BA129	32 Kwords	3D0000h-3D7FFFh
	BA128	32 Kwords	3C8000h-3CFFFFh
	BA127	32 Kwords	3C0000h-3C7FFFh
	BA126	32 Kwords	3B8000h-3BFFFFh
	BA125	32 Kwords	3B0000h-3B7FFFh
	BA124	32 Kwords	3A8000h-3AFFFFh
	BA123	32 Kwords	3A0000h-3A7FFFh
	BA122	32 Kwords	398000h-39FFFFh
	BA121	32 Kwords	390000h-397FFFh
	BA120	32 Kwords	388000h-38FFFFh
	BA119	32 Kwords	380000h-387FFFh
	BA118	32 Kwords	378000h-37FFFFh
	BA117	32 Kwords	370000h-377FFFh
	BA116	32 Kwords	368000h-36FFFFh
	BA115	32 Kwords	360000h-367FFFh
	BA114	32 Kwords	358000h-35FFFFh
	BA113	32 Kwords	350000h-357FFFh
	BA112	32 Kwords	348000h-34FFFFh
	BA111	32 Kwords	340000h-347FFFh
	BA110	32 Kwords	338000h-33FFFFh
	BA109	32 Kwords	330000h-337FFFh
	BA108	32 Kwords	328000h-32FFFFh
	BA107	32 Kwords	320000h-327FFFh
	BA106	32 Kwords	318000h-31FFFFh
	BA105	32 Kwords	310000h-317FFFh
	BA104	32 Kwords	308000h-30FFFFh
	BA103	32 Kwords	300000h-307FFFh
	BA102	32 Kwords	2F8000h-2FFFFFh
	BA101	32 Kwords	2F0000h-2F7FFFh
	BA100	32 Kwords	2E8000h-2EFFFFh
	BA99	32 Kwords	2E0000h-2E7FFFh
	BA98	32 Kwords	2D8000h-2DFFFFh
	BA97	32 Kwords	2D0000h-2D7FFFh
	BA96	32 Kwords	2C8000h-2CFFFFh
	BA95	32 Kwords	2C0000h-2C7FFFh
	BA94	32 Kwords	2B8000h-2BFFFFh
	BA93	32 Kwords	2B0000h-2B7FFFh
	BA92	32 Kwords	2A8000h-2AFFFFh

Table 13. Block Architecture

Bank	Block	Block Size	(x16) Address Range
Bank 1	BA91	32 Kwords	2A0000h-2A7FFFh
	BA90	32 Kwords	298000h-29FFFFh
	BA89	32 Kwords	290000h-297FFFh
	BA88	32 Kwords	288000h-28FFFFh
	BA87	32 Kwords	280000h-287FFFh
	BA86	32 Kwords	278000h-27FFFFh
	BA85	32 Kwords	270000h-277FFFh
	BA84	32 Kwords	268000h-26FFFFh
	BA83	32 Kwords	260000h-267FFFh
	BA82	32 Kwords	258000h-25FFFFh
	BA81	32 Kwords	250000h-257FFFh
	BA80	32 Kwords	248000h-24FFFFh
	BA79	32 Kwords	240000h-247FFFh
	BA78	32 Kwords	238000h-23FFFFh
	BA77	32 Kwords	230000h-237FFFh
	BA76	32 Kwords	228000h-22FFFFh
	BA75	32 Kwords	220000h-227FFFh
	BA74	32 Kwords	218000h-21FFFFh
	BA73	32 Kwords	210000h-217FFFh
	BA72	32 Kwords	208000h-20FFFFh
	BA71	32 Kwords	200000h-207FFFh
	BA70	32 Kwords	1F8000h-1FFFFFh
	BA69	32 Kwords	1F0000h-1F7FFFh
	BA68	32 Kwords	1E8000h-1EFFFFh
	BA67	32 Kwords	1E0000h-1E7FFFh
	BA66	32 Kwords	1D8000h-1DFFFFh
	BA65	32 Kwords	1D0000h-1D7FFFh
	BA64	32 Kwords	1C8000h-1CFFFFh
	BA63	32 Kwords	1C0000h-1C7FFFh
	BA62	32 Kwords	1B8000h-1BFFFFh
	BA61	32 Kwords	1B0000h-1B7FFFh
	BA60	32 Kwords	1A8000h-1AFFFFh
	BA59	32 Kwords	1A0000h-1A7FFFh
	BA58	32 Kwords	198000h-19FFFFh
	BA57	32 Kwords	190000h-197FFFh
	BA56	32 Kwords	188000h-18FFFFh
	BA55	32 Kwords	180000h-187FFFh
	BA54	32 Kwords	178000h-17FFFFh
	BA53	32 Kwords	170000h-177FFFh
	BA52	32 Kwords	168000h-16FFFFh
	BA51	32 Kwords	160000h-167FFFh
	BA50	32 Kwords	158000h-15FFFFh
	BA49	32 Kwords	150000h-157FFFh
	BA48	32 Kwords	148000h-14FFFFh
	BA47	32 Kwords	140000h-147FFFh

Table 13. Block Architecture

Bank	Block	Block Size	(x16) Address Range
Bank 1	BA46	32 Kwords	138000h-13FFFFh
	BA45	32 Kwords	130000h-137FFFh
	BA44	32 Kwords	128000h-12FFFFh
	BA43	32 Kwords	120000h-127FFFh
	BA42	32 Kwords	118000h-11FFFFh
	BA41	32 Kwords	110000h-117FFFh
	BA40	32 Kwords	108000h-10FFFFh
	BA39	32 Kwords	100000h-107FFFh
Bank 0	BA38	32 Kwords	0F8000h-0FFFFFh
	BA37	32 Kwords	0F0000h-0F7FFFh
	BA36	32 Kwords	0E8000h-0EFFFFh
	BA35	32 Kwords	0E0000h-0E7FFFh
	BA34	32 Kwords	0D8000h-0DFFFFh
	BA33	32 Kwords	0D0000h-0D7FFFh
	BA32	32 Kwords	0C8000h-0CFFFFh
	BA31	32 Kwords	0C0000h-0C7FFFh
	BA30	32 Kwords	0B8000h-0BFFFFh
	BA29	32 Kwords	0B0000h-0B7FFFh
	BA28	32 Kwords	0A8000h-0AFFFFh
	BA27	32 Kwords	0A0000h-0A7FFFh
	BA26	32 Kwords	098000h-09FFFFh
	BA25	32 Kwords	090000h-097FFFh
	BA24	32 Kwords	088000h-08FFFFh
	BA23	32 Kwords	080000h-087FFFh
	BA22	32 Kwords	078000h-07FFFFh
	BA21	32 Kwords	070000h-077FFFh
	BA20	32 Kwords	068000h-06FFFFh
	BA19	32 Kwords	060000h-067FFFh
	BA18	32 Kwords	058000h-05FFFFh
	BA17	32 Kwords	050000h-057FFFh
	BA16	32 Kwords	048000h-04FFFFh
	BA15	32 Kwords	040000h-047FFFh
	BA14	32 Kwords	038000h-03FFFFh
	BA13	32 Kwords	030000h-037FFFh
	BA12	32 Kwords	028000h-02FFFFh
	BA11	32 Kwords	020000h-027FFFh
	BA10	32 Kwords	018000h-01FFFFh
	BA9	32 Kwords	010000h-017FFFh
	BA8	32 Kwords	008000h-00FFFFh
	BA7	4 Kwords	007000h-007FFFh
	BA6	4 Kwords	006000h-006FFFh
	BA5	4 Kwords	005000h-005FFFh
	BA4	4 Kwords	004000h-004FFFh
	BA3	4 Kwords	003000h-003FFFh
	BA2	4 Kwords	002000h-002FFFh
	BA1	4 Kwords	001000h-001FFFh
	BA0	4 Kwords	000000h-000FFFh

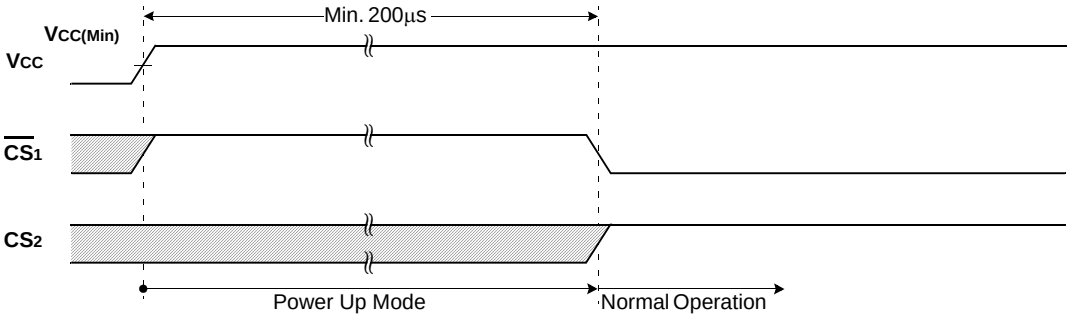
32Mb(2M x16) C-die

Page Mode UtRAM

POWER UP SEQUENCE

1. Apply power.
2. Maintain stable power(Vcc min.=2.7V) for a minimum 200μs with $\overline{CS}$1=high.or CS2=low.

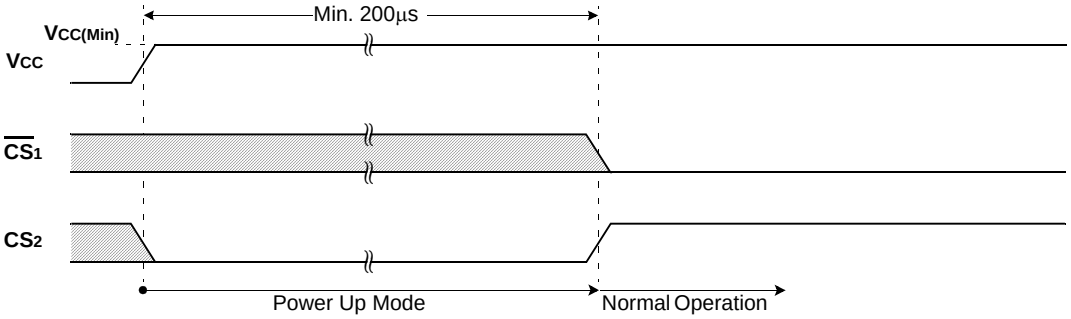
TIMING WAVEFORM OF POWER UP(1) ($\overline{CS}_1$ controlled)



POWER UP(1)

1. After V_{CC} reaches V_{CC}(Min.), wait 200μs with $\overline{CS}_1$ high. Then the device gets into the normal operation.

TIMING WAVEFORM OF POWER UP(2) (CS_2 controlled)



POWER UP(2)

1. After V_{CC} reaches V_{CC}(Min.), wait 200μs with CS_2 low. Then the device gets into the normal operation.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1~8	I/O9~16	Mode	Power
H	X[1]	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
X[1]	L	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
X[1]	X[1]	X[1]	X[1]	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X[1]	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X[1]	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X[1]	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X[1]	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X[1]	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS[1]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CC}+0.3V	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 3.6V	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-25 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	2.7	2.9	3.1	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.3[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.6	V

1. T_A=-25 to 85°C, otherwise specified.
2. Overshoot: Vcc+1.0V in case of pulse width ≤20ns.
3. Undershoot: -1.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)](f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

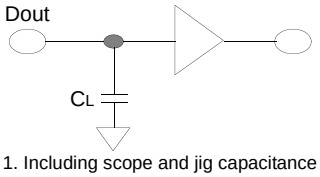
Item	Symbol	Test Conditions	Min	Typ[1)]	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc	-1	-	1	μA
Output leakage current	I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{LB}$=$\overline{UB}$=V_{IH}, V_{IO}=Vss to Vcc	-1	-	1	μA
Average operating current	I_{CC1}	Cycle time=1μs, 100% duty, I_{IO}=0mA, $\overline{CS1}$≤0.2V, $\overline{LB}$≤0.2V or/and $\overline{UB}$≤0.2V, CS_2≥Vcc-0.2V, V_{IN}≤0.2V or V_{IN}≥Vcc-0.2V	-	-	7	mA
	I_{CC2}	Cycle time=Min, I_{IO}=0mA, 100% duty, $\overline{CS1}$=V_{IL}, CS_2=V_{IH}, $\overline{LB}$=V_{IL} or/and $\overline{UB}$=V_{IL},V_{IN}=V_{IL} or V_{IH}	-		35	mA
Output low voltage	V_{OL}	I_{OL}=2.1mA	-	-	0.4	V
Output high voltage	V_{OH}	I_{OH}=-1.0mA	2.4	-	-	V
Standby Current(CMOS)	I_{SB1}[2)]	Other inputs = 0~Vcc 1) $\overline{CS_1}$≥Vcc-0.2V, CS_2≤Vcc-0.2V ($\overline{CS_1}$ controlled) or 2) 0V≤CS_2≤0.2V(CS_2 controlled)	-	-	100	μA

1. Typical values are tested at V_{CC}=2.9V, T_A=25°C and not guaranteed.
2. I_{SB1} is measured after 60ms from the time when standby mode is set up.

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.2V
Input rising and falling time: 5ns
Input and output reference voltage: 1.5V
Output load: C_L=50pF



1. Including scope and jig capacitance

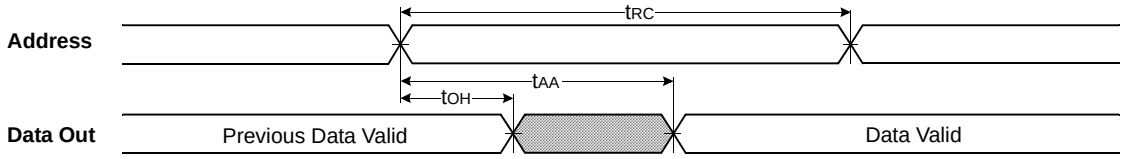
AC CHARACTERISTICS(V_{CC}=2.7~3.1V, T_A=-25 to 85°C)

Parameter List		Symbol	Speed Bin		Units
			70ns[1]		
			Min	Max	
Read	Read Cycle Time	t_{RC}	70	-	ns
	Address Access Time	t_{AA}	-	70	ns
	Chip Select to Output	t_{CO}	-	70	ns
	Output Enable to Valid Output	t_{OE}	-	35	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	70	ns
	Chip Select to Low-Z Output	t_{LZ}	10	-	ns
	$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	t_{BLZ}	10	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	ns
	Chip Disable to High-Z Output	t_{HZ}	0	25	ns
	$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	25	ns
	Output Disable to High-Z Output	t_{OHZ}	0	25	ns
	Output Hold from Address Change	t_{OH}	3	-	ns
	Page Cycle	t_{PC}	25	-	ns
	Page Access Time	t_{PA}	-	20	ns
Write	Write Cycle Time	t_{WC}	70	-	ns
	Chip Select to End of Write	t_{CW}	60	-	ns
	Address Set-up Time	t_{AS}	0	-	ns
	Address Valid to End of Write	t_{AW}	60	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	60	-	ns
	Write Pulse Width	t_{WP}	55[1]	-	ns
	Write Recovery Time	t_{WR}	0	-	ns
	Write to Output High-Z	t_{WHZ}	0	25	ns
	Data to Write Time Overlap	t_{DW}	30	-	ns
	Data Hold from Write Time	t_{DH}	0	-	ns
	End Write to Output Low-Z	t_{OW}	5	-	ns

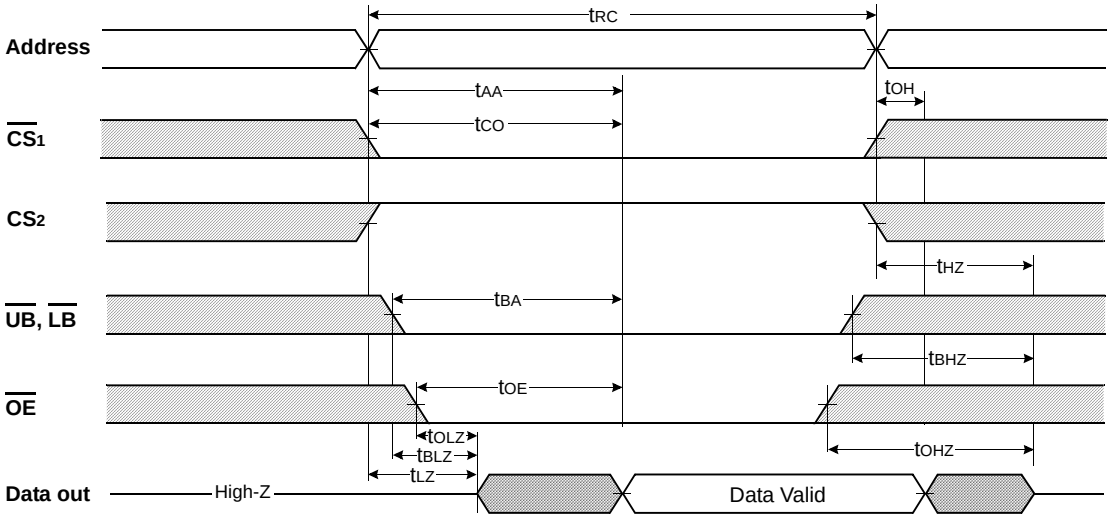
1. t_{WC}(min)=90ns or t_{WP}(min)=70ns for continuous write operation over 50 times.

TIMING DIAGRAMS

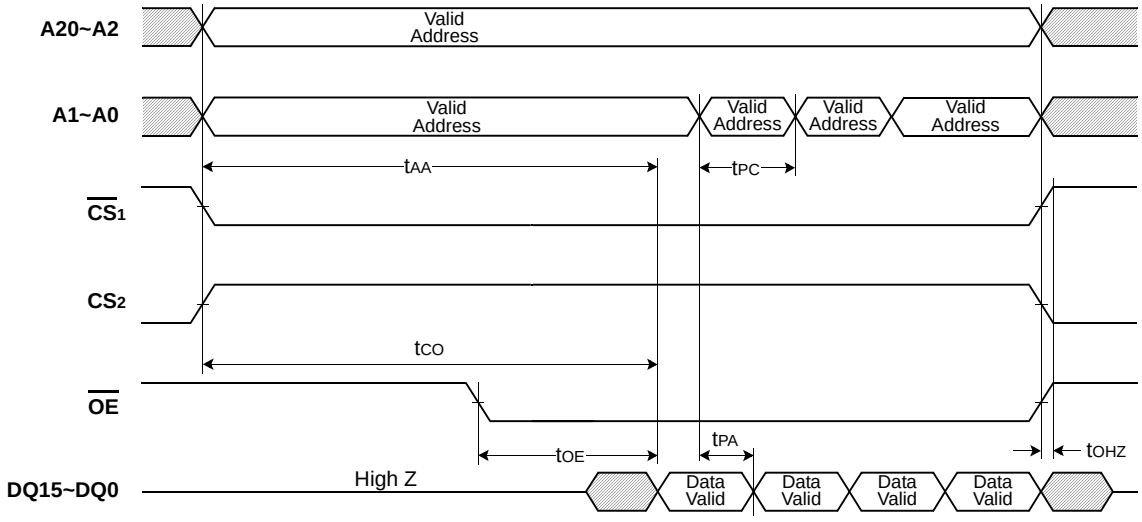
TIMING WAVEFORM OF READ CYCLE(1)(Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, $\overline{UB}$ or/and $\overline{LB}$=V_{IL})



TIMING WAVEFORM OF READ CYCLE(2)($\overline{WE}$=V_{IH})



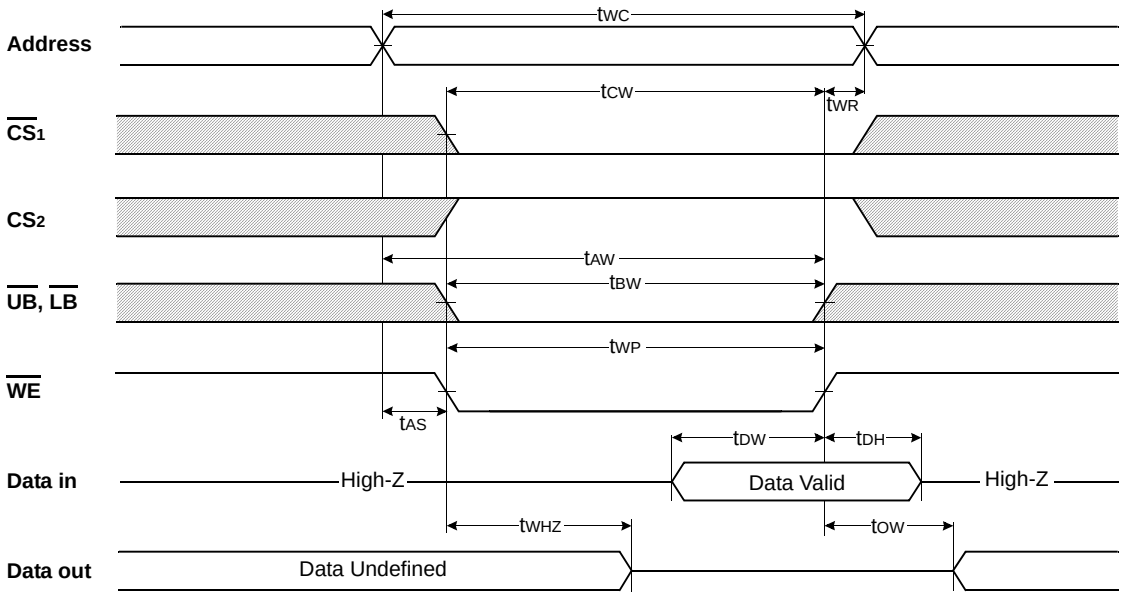
TIMING WAVEFORM OF PAGE CYCLE(READ ONLY)



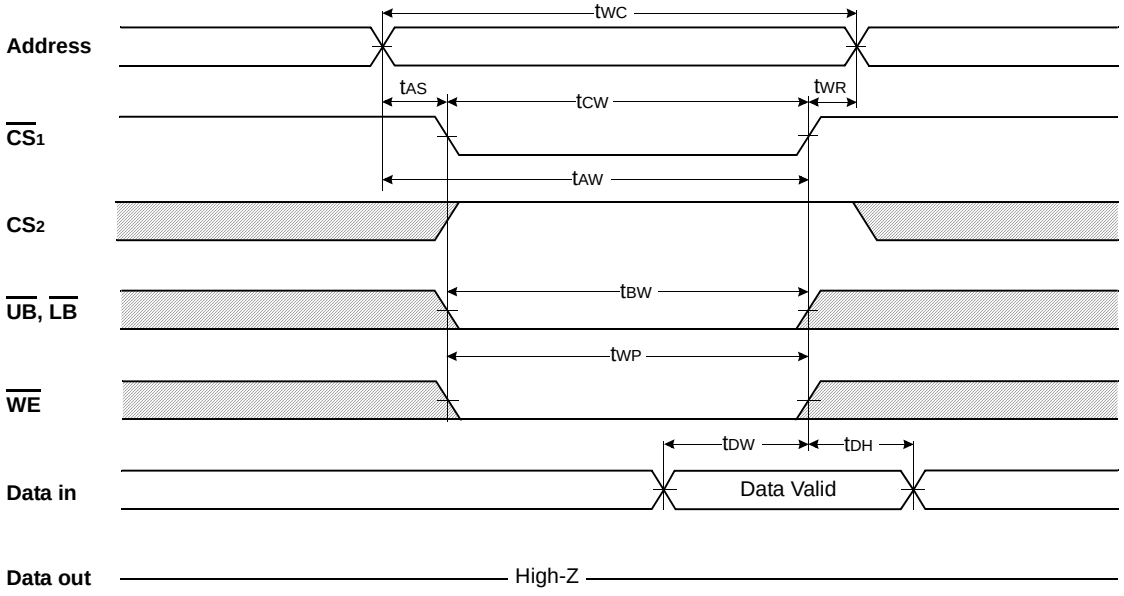
(READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.
3. t_{OE}(max) is met only when $\overline{OE}$ becomes enabled after t_{AA}(max).
4. If invalid address signals shorter than min. t_{RC} are continuously repeated for over 4us, the device needs a normal read timing(t_{RC}) or needs to sustain standby state for min. t_{RC} at least once in every 4us.

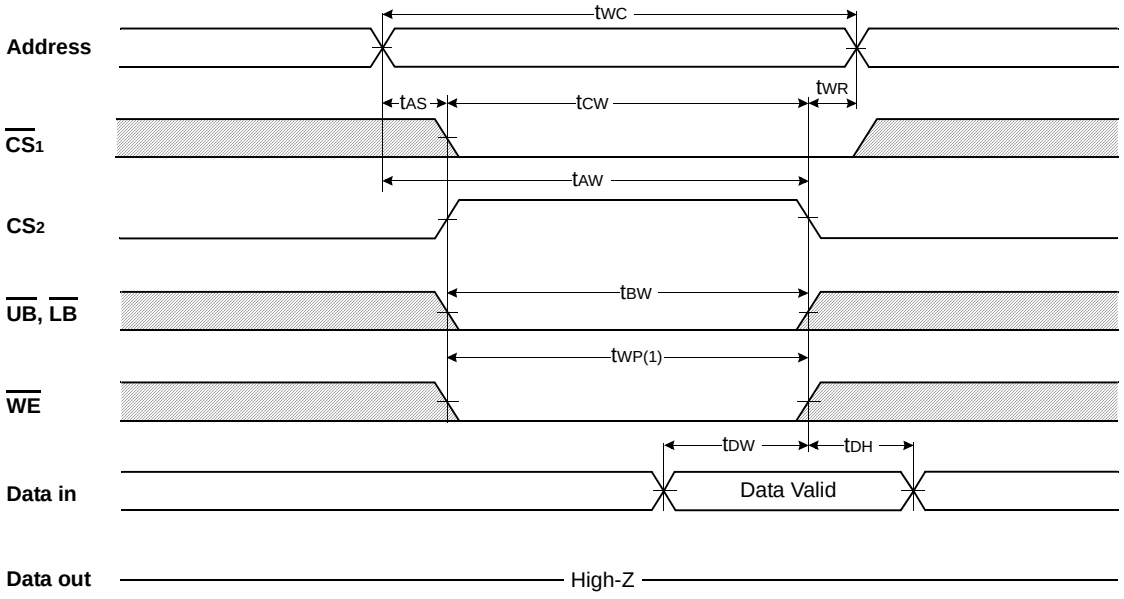
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



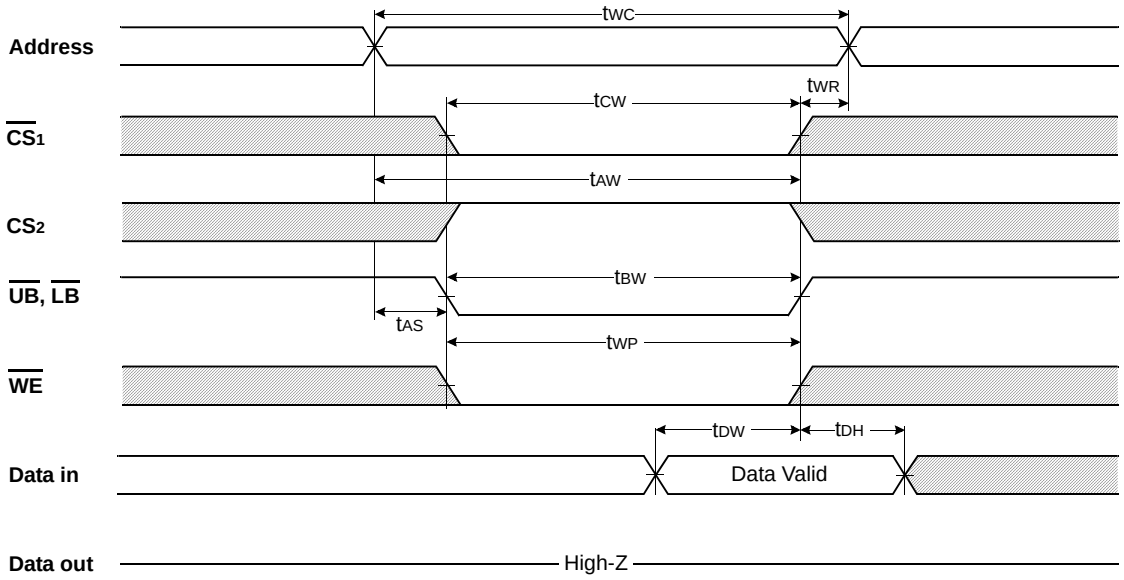
TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS_2 Controlled)



TIMING WAVEFORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS_1}$ and low $\overline{WE}$. A write begins when $\overline{CS_1}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS_1}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS_1}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS_1}$ or $\overline{WE}$ going high.

PACKAGE DIMENSION

64-Ball Fine pitch Ball Grid Array Package (measured in millimeters)